

 ICOM

# SERVICE MANUAL

COMMUNICATIONS RECEIVER  
**IC-R75**

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## INTRODUCTION

This service manual describes the latest service information for the IC-R75 at the time of publication.

VERSION	SYMBOL
U.S.A.	USA
Europe	EUR
U.K.	UK
S.E.Asia	SEA
Other	OTH

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

## DANGER

**NEVER** connect the receiver to an AC outlet or to a DC power supply that uses more than 16 V. Such a connection could cause a fire hazard and/or electric.

**DO NOT** expose the receiver to rain, snow or any liquids.

**DO NOT** reverse the polarities of the power supply when connecting the receiver.

**DO NOT** apply an RF signal of more than 20 dBm (100mW) to the antenna connector. This could damage the receiver's front end.



## ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

### <SAMPLE ORDER>

0910051123 PCB	B-5274C	IC-R75	PLL UNIT	1 pieces
8810005770 Screw	Bih M3x8 ZK	IC-R75	Chassis	10 pieces

Addresses are provided on the inside back cover for your convenience.

## REPAIR NOTES

1. Make sure a problem is internal before disassembling the receiver.
2. **DO NOT** open the receiver until the receiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the receiver is defective.
6. **READ** the instructions of test equipment thoroughly before connecting equipment to the receiver.

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# SECTION 1      SPECIFICATIONS

## ■ GENERAL

- Frequency range

Version	Frequency coverage
USA, EUR, UK, OTH	30 kHz – 60 MHz <sup>*1</sup>
SEA	30 kHz – 30 MHz <sup>*2</sup>

<sup>\*1</sup> Specifications guaranteed for 0.1 – 29.99 MHz and 50 – 54 MHz

<sup>\*2</sup> Specifications guaranteed for 0.1 – 29.99 MHz

- Mode : SSB (LSB, USB), AM, FM, CW, RTTY, S-AM

- Receive system : Triple-conversion superheterodyne

- Intermediate frequencies

	SSB	CW	RTTY	AM, S-AM	FM
1st (MHz)	69.0115	69.0106	69.0105	69.0100	69.0115
2nd (MHz)	9.0115	9.0106	9.0105	9.0100	9.0115
3rd (MHz)	0.4550	0.4559	0.4560	0.4500	0.4500

May differ according to selected IF filter.

- Sensitivity

0.1 MHz – 1.799 MHz (Preamplifiers are OFF)	
SSB, CW, RTTY	less than 2.0 µV for 10 dB S/N
AM, S-AM	less than 13.0 µV for 10 dB S/N
1.8 MHz – 27.99 MHz (The preamplifier 1 is ON)	
SSB, CW, RTTY	less than 0.16 µV for 10 dB S/N (typical)
AM, S-AM	less than 2.0 µV for 10 dB S/N
28 MHz – 29.99 MHz (The preamplifier 1 is ON)	
SSB, CW, RTTY	less than 0.16 µV for 10 dB S/N (typical)
AM, S-AM	less than 2.0 µV for 10 dB S/N
FM	less than 0.5 µV for 12 dB SINAD
50 MHz – 54 MHz (The preamplifier 2 is ON)	
SSB, CW, RTTY	less than 0.13 µV for 10 dB S/N (typical)
AM, S-AM	less than 1.0 µV for 10 dB S/N
FM	less than 0.25 µV for 12 dB SINAD

- selectivity

SSB, CW, RTTY	More than 2.1 kHz/-6 dB Less than 4.0 kHz/-60 dB
AM, S-AM	More than 6.0 kHz/-6 dB less than 20.0 kHz/-50 dB
FM	More than 12.0 kHz/-6 dB less than 30.0 kHz/-40 dB

- Audio output power

: More than 2.0 W at 10 % distortion with an 8 Ω load

- Antenna impedance

: 50 Ω or 450 Ω

- Squelch sensitivity (threshold) :

Frequency (MHz)	SSB	FM
0.1 – 1.799	less than 71 µV*	–
1.8 – 27.99	less than 5.6 µV <sup>*1</sup>	–
28 – 29.99	–	less than 0.32 µV <sup>*1</sup>
50 – 54	less than 5.6 µV <sup>*2</sup>	less than 0.32 µV <sup>*2</sup>

\*Preamplifiers are OFF; <sup>\*1</sup>Preamplifier 1 is ON; <sup>\*2</sup>Preamplifier 2 is ON

- Current drain (13.8 V DC)

: Less than 1.3 A (Standby), Less than 1.5 A (Max. audio out)

- Spurious and image rejection

: More than 70 dB (0.1 – 1.799 MHz SSB, AM, S-AM are more than 60 dB)

- Dimensions

: 241(W)×94(H)×229(D) mm; 9½(W)×31½(H)×9½(D) inch (projection not included)

- Weight (approximate)

: 3.0 kg; 6 lb 10 oz (AC adaptor "AD-55/A/V" is not included)

- Antenna connector

: SO-239 (50 Ω), push connection terminal (450 Ω)

- CI-V connector

: 2-connector 3.5 (d) mm (1/8")/8 Ω

- PHONES connector

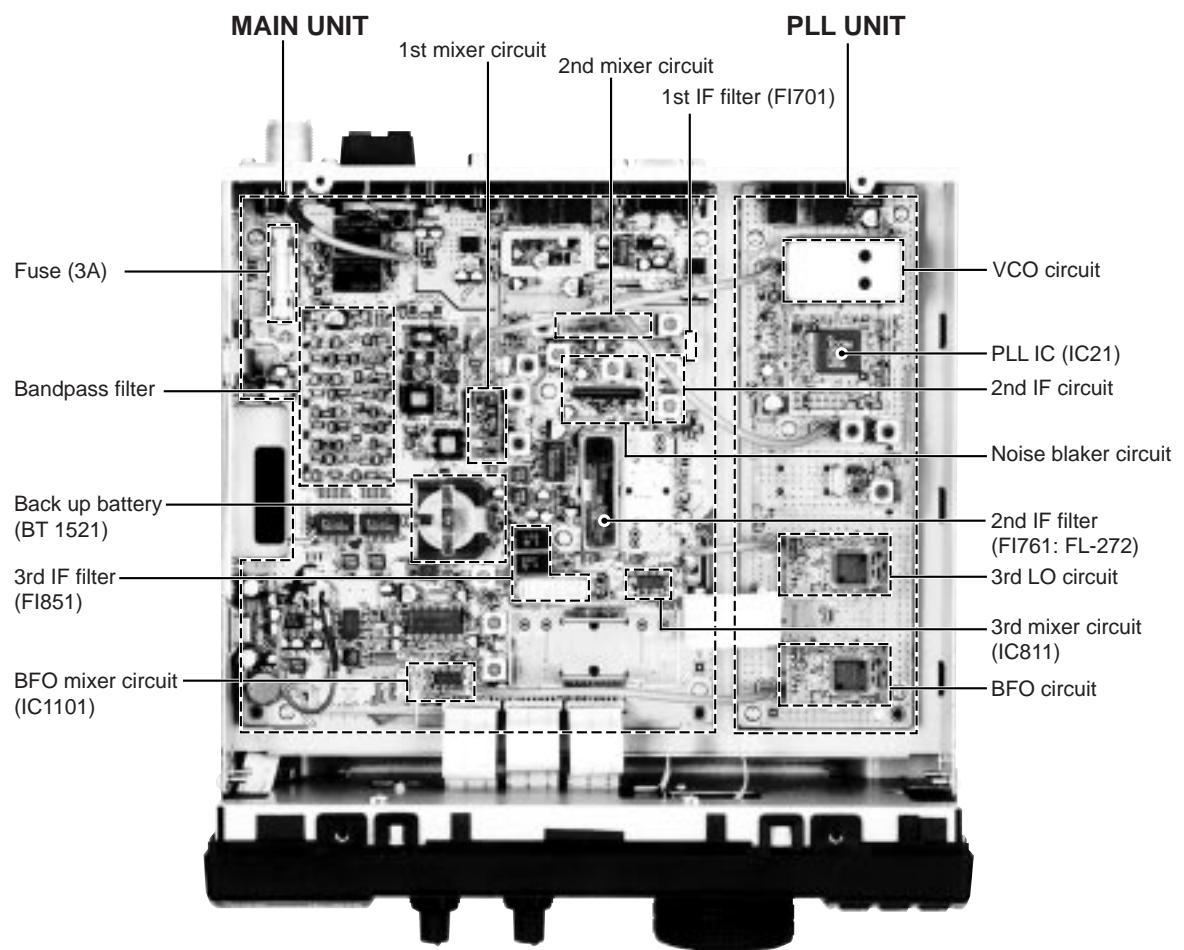
: 3-conductor 6.35 (d) mm (1/8")

- External speaker connector

: 2-conductor 3.5 (d) mm (1/8")/8 Ω

All stated specifications are subject to change without notice or obligation.

## SECTION 2     INSIDE VIEWS



## SECTION 3 CIRCUIT DESCRIPTION

### 3-1 RECEIVER CIRCUITS

#### 3-1-1 RF SWITCHING CIRCUIT (MAIN UNIT)

The IC-R75 has two antenna connectors. RF signals enter either the [50 Ω ANT.] or [450 Ω ANT.] connector.

RF signals from the [50 Ω ANT.] connector are applied to the antenna switching circuit (RL121), and then pass through the low-pass filter (L131, L132, C131–C136).

RF signals from the [450 Ω ANT.] connector are passed through the L101 to exchange the impedance value, and are then applied to the antenna switching circuit (RL121). The signals are applied to the low-pass filter (L131, L132, C131–C136).

Each RF signals from the [50 Ω ANT.] connector or [450 Ω ANT.] connector are chosen by the antenna switching circuit (RL121).

#### 3-1-2 RF FILTER CIRCUIT (MAIN UNIT)

The filtered signals are applied to the RX attenuator switching circuit (RL141). Either the signals bypass or pass through the attenuator circuit. The signals are attenuated at 20 dB when passing through the attenuators. The attenuator system excludes non-linear components between an antenna connector and an attenuator to prevent strong signals from causing distortion. The signals are then applied to the RF filters. The MAIN UNIT has 8 RF bandpass filters for signals above 2.0 MHz and 2 low-pass filters for signals below 2.0 MHz.

#### (1) Below 1.6 MHz

The signals are applied to the low-pass filter consisting of C170–C175, L171–L173 via the limitter circuit (D141, D142). A diode is removed at the entrance of the low-pass filter. This device prevents the diode from causing distortion when receiving very strong signals. A switching diode (D172) is turned on when the "B0" line is "HIGH".

#### (2) Above 1.6 MHz

The signals are applied to the high-pass filter consisting of C161–C163, L161–L164. This filter suppresses strong signals below 1.6 MHz such as broadcasting stations.

The filtered signal between 1.6 MHz and 2.0 MHz are applied to the low-pass filter (C182–C187, L182, L183) via the switching diode (D181). The switching diodes (D181, D182) are turned ON when the "B1" line is "HIGH".

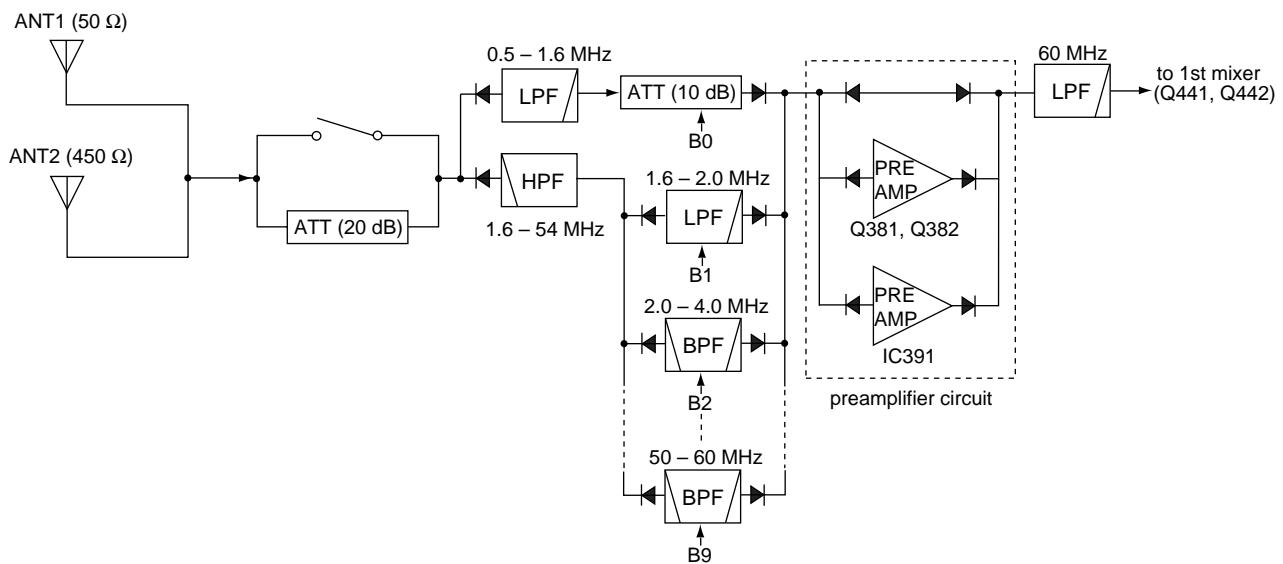
The filtered signals above 2.0 MHz are applied to one of 8 bandpass filters depending on the receive frequencies.

After passing through a bandpass or low-pass filter, the signals are applied to the pre-amplifier circuit (Q381, Q382, IC391).

#### (3) FILTER SWITCHING CIRCUIT

The RF bandpass filter corresponds to the BPF switching voltage (B0–B9) based on the CPU via the shift register (IC551, IC552) and driver (IC561, IC562). The switching voltage of the BPF exit to improve multi-signal and strong signal characteristics.

- RF bandpass and preamplifier circuit



### 3-1-3 PRE-AMPLIFIER CIRCUIT (MAIN UNIT)

The pre-amplifier circuit uses low noise junction FETs (Q381, Q382) or wideband amplifier (IC391) to provide gain over a wide frequency range.

When the [P.AMP] switch is turned "PREAMP 1", the signals from the RF filter are amplified by the junction FETs pre-amplifier circuit (Q381, Q382).

When the [P.AMP] switch is turned "PREAMP 2", the signals from the RF filter are amplified by the wideband pre-amplifier circuit (IC391).

When the [P.AMP] switch is turned "PREAMP OFF", the signals from the RF filter bypass the pre-amplifiers through D371 and D372.

The amplified or bypassed signals are applied to the 1st mixer circuit (Q441, Q442) via the low-pass filter (L431, L432 and C431–CC436). The low-pass filter attenuates at 50 MHz to suppress image frequency.

### 3-1-4 1ST MIXER AND IF CIRCUITS (MAIN UNIT)

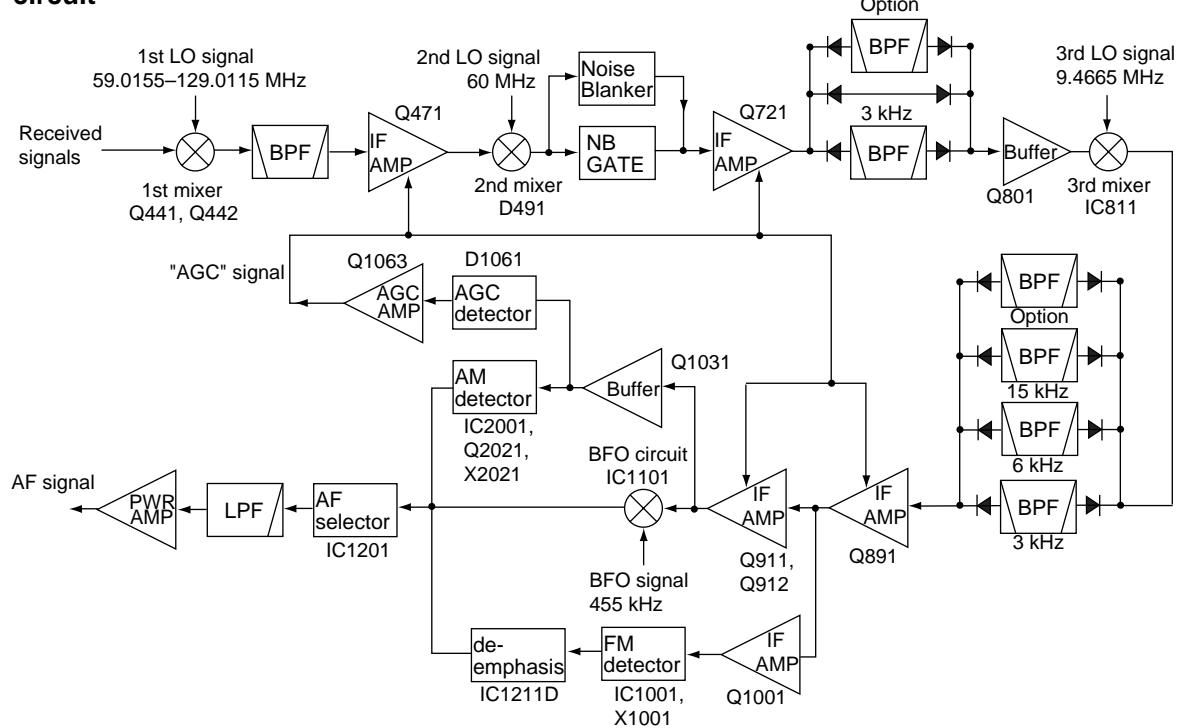
The filtered signals are mixed with a 69.0415–129.0115 MHz 1st LO signal to produce a 69.01 MHz 1st IF signal at the 1st mixer circuit (Q441, Q442).

#### 1ST IF FREQUENCY

MODE	FREQUENCY
LSB, USB, FM	69.0115 MHz
CW	69.0106 MHz
RTTY	69.0105 MHz
AM, S-AM	69.0100 MHz

The 1st mixer circuit employs a balanced mixer using low-noise junction FETs (Q441, Q442) to expand the dynamic range.

#### • IF circuit



The 69.0415–129.0115 MHz 1st LO signal is applied to an LO amplifier (Q411) from the PLL unit via J411, and then passes through the low-pass filter (L421, L422, C422–C425). The filtered signal is applied to the 1st mixer circuit.

The 1st IF signal is applied to the crystal bandpass filter(FI-461) to suppress out-of-band signals. The filtered signal is amplified at a 1st IF amplifier (Q471), and then applied to a 2nd mixer circuit (D491)

### 3-1-5 2ND MIXER AND IF CIRCUITS (MAIN UNIT)

The 1st IF signal is mixed with a 60.0 MHz 2nd LO signal to produce 9 MHz 2nd IF signal at the 2nd mixer (D491, C492, L491, L492). The 60.0 MHz 2nd LO signal is applied to the 2nd mixer from the PLL unit via J491.

#### 2ND IF FREQUENCY

MODE	FREQUENCY
LSB, USB, FM	9.0115 MHz
CW	9.0106 MHz
RTTY	9.0105 MHz
AM, S-AM	9.0100 MHz

The 9 MHz 2nd IF signal is applied to the crystal bandpass filter (FI701) to suppress unwanted signals.

The filtered signal enters the noise blanker gate (D711–D714). The signal is applied to L712 to obtain clear reception and is then amplified at the 2nd IF amplifier (Q721). The signal passes through a loose resonator circuit (C726, L721) and then is applied to one of the two crystal bandpass filters.

When the [FIL] switch is turned “2F3K”, the filter is selected FI761 which covering the 2.4 kHz bandwith.

When the [FIL] switch is turned “2FOP”, the filter is selected an optional filter.

When the [FIL] switch is turned “2FTH”, the signal from the 2nd IF amplifier bypass the crystal bandpass filters through D771 and D773.

The filtered or bypassed signal is amplified at the buffer amplifier (Q801) and applied to the 3rd mixer circuit (IC811).

### 3-1-6 NOISE BLANKER CIRCUITS (MAIN UNIT)

The IC-R75 uses a trigger noise blanker circuit which removes pulse-type noise signals at the noise blanker gate (D711–D714).

The 2nd IF signal passes through the crystal bandpass filter (FI701) to suppress unwanted signals. A portion of the output signal is applied to a noise amplifier circuit (IC731, Q731, Q733) and detected at a noise detector circuit (D731). The detected voltage is applied to a noise blanker gate control circuit (Q735–Q737, D732).

The threshold level of the noise blanker gate control circuit (Q735–Q737, D732) is set at 1.0 V on SSB mode (In case of AM mode, is set at 1.6 V). When the detected voltage exceeds the threshold level, Q737 outputs a blanking signal to activate the noise blanker gate (D711–D714).

A portion of the detected voltage is applied to the noise blanker AGC circuit (Q732, Q734). The noise components are fed back to the noise amplifier (IC731). The time constant of the noise blanker AGC circuit is determined by R737, R744 and C739. This AGC circuit does not operate to detect pulse-type noise.

When the operating frequency or mode is changed, the “UNLC” signal is applied to the noise blanker gate control circuit (D732). The noise blanker gate prevents PLL click noise.

### 3-1-7 3RD MIXER AND IF CIRCUITS (MAIN UNIT)

The 2nd IF signal is mixed with a 9.4665 MHz 3rd LO signal to produce a 450–456 kHz 3rd IF signal at the 3rd mixer (IC811).

#### 3RD IF FREQUENCY

MODE	FREQUENCY
LSB, USB	455.0 kHz
CW	455.9 kHz
RTTY	456.0 kHz
AM, S-AM	450.0 kHz

The 9.4665 MHz 3rd LO signal is applied to the 3rd mixer IC (IC811, pin 10) from the PLL unit via J811. The 450–456 kHz 3rd IF signal is applied either to one of the 3 ceramic bandpass filters (FI851, FI861, FI871) or to an optional crystal bandpass filter to suppress unwanted signals.

When the [FIL] switch is turned “3F3K”, the filter is selected FI851 which covering the 2.4 kHz bandwith.

When the [FIL] switch is turned “3F6K”, the filter is selected FI861 which covering the 6 kHz bandwith.

When the [FIL] switch is turned “3F15”, the filter is selected FI871 which covering the 15 kHz bandwith.

When the [FIL] switch is turned “3FOP”, the filter is selected an optional crystal bandpass filter.

When the mode is selected SSB mode, the filtered 3rd IF signal is amplified at the 3rd IF amplifier (Q891), and is then applied to the 3rd IF amplifier (Q911) via the receiver total gain control circuit (R898). The amplified signal is applied to the SSB demodulator circuit.

When the mode is selected FM mode, the filtered 3rd IF signal is amplified at the 3rd IF amplifier (Q891), and is then applied to the FM demodulator circuit.

When the mode is selected AM mode, the filtered 3rd IF signal is amplified at the 3rd IF amplifier (Q891), and is then applied to the 3rd IF amplifier (Q911) via the receiver total gain control circuit (R898). The amplified signal is applied to the AM demodulator circuit.

1st, 2nd and 3rd IF amplifiers (Q471, Q721, Q891) are controlled by AGC bias voltage.

### 3-1-8 BFO CIRCUIT (PLL UNIT)

The BFO (Beat Frequency Oscillator) circuit consists of Q1, X1, Q201 and IC 201 on PLL unit. The oscillator provides a beat frequency signal to the SSB demodulator circuit (MAIN UNIT; IC1101) for demodulating the 3rd IF signal into an AF signal.

The 30 MHz signal is oscillated at Q1 and X1 for the system clock signal of the DDS IC (IC201). The oscillated signal is amplified at Q201 and is applied to the DDC IC (IC201, pin 7) to produce the 455 kHz BFO signal.

The 455 kHz signal passes through the low-pass filter (L201, L202, C202–C207) via the D/A converter, and is then mixed with the 3rd IF signal at the SSB demodulator circuit (MAIN unit; IC1101).

### 3-1-9 DEMODULATOR CIRCUIT (MAIN UNIT)

The demodulator circuit consists of 3 detector circuits.

#### (1) SSB DEMODULATOR CIRCUIT

A product detector (IC1101) demodulates SSB, RTTY and CW signals into an AF signal. The 3rd IF signal from the IF amplifier (Q911) is mixed with the BFO signal at the product detector (IC1101) to be demodulated into an AF signal. The AF signal passes through the AF input mode selector switch (IC1201).

#### (2) FM DEMODULATOR CIRCUIT

A FM detector (IC1001, X1001) demodulates the FM signal into an AF signal. The 3rd IF signal from the IF amplifier (Q891) is amplified at the 3rd IF amplifier (Q1001), and is then applied to the FM detector (IC1001, X1001) to demodulate the 3rd IF signal. The demodulated signal is applied to the de-emphasis circuit (IC1211D) to produce the FM AF signal. The AF signal passes through the AF input mode selector switch (IC1201).

The FM detector outputs "FMNL" signal from IC1001, pin 14 is applied to the CPU (LOGIC unit; IC101, pin 94) to control the noise squelch level.

### (3) AM DEMODULATOR CIRCUIT

The AM demodulator circuit (IC2001) has the envelope detect function and the synchronous detect function. An AM detector (IC2001) demodulates the AM signal into an AF signal. The 3rd IF signal from the IF amplifier (Q911) is amplified at the buffer amplifier (Q1031), and is then applied to the AM demodulator circuit (IC2001) to demodulate the 3rd IF signal into the AM AF signal. The AF signal which is the AM envelope detect the AF signal or the AM synchronous detect AF signal passes through the AF input mode selector switch (IC1201).

### 3-1-10 AF INPUT MODE SELECTOR SWITCH (MAIN AND LOGIC UNITS)

The AF input mode selector switch (MAIN unit; IC1201) consists of 4 analog switches. The switches are selected mode signals of "AFS1" and "AFS2" from the CPU (LOGIC unit; IC101) via the shift register (MAIN unit; IC1601), and are selected by the squelch control signal from the CPU (LOGIC unit; IC101). The AF signal is output from IC1201 (MAIN unit; pin 13).

### 3-1-11 AF AMPLIFIER CIRCUIT (MAIN AND FRONT UNITS)

The AF signal output is passed through the low-pass filter (IC1211) to suppress unwanted signals. The filtered signal is mixed with "BEEP" signal at the AF level variable circuit (MAIN unit; IC1251), and is then applied to the AF amplifier circuit and the AF level variable circuit (IC1251).

The AF level variable circuit controls the AF level by the "AF GAIN" (R141) on the VR BOARD. The AF signal is applied to the AF mute circuit to suppress the noise when "AF GAIN" (R141) level is minimum, and is then power-amplified at IC1291 on the MAIN unit to drive the speaker.

The one of the AF amplified signal is output "AAFO" signal to record the AF signal to the AF recording jack (PLL unit; J3).

### 3-1-12 AGC AND S-METER CIRCUITS (MAIN UNIT)

The AGC (Automatic Gain Control) circuit reduces signal fading and keep the audio output level constant. The receiver gain is determined by voltage on the AGC line (Q1063, collector). When strong signals are received, the AGC circuit decreases the voltage on this line.

The 3rd IF signal is amplified at the IF amplifier (Q911). A portion of the 3rd IF signal is applied to the buffer amplifier (Q1031) to convert the impedance. The amplified IF signal is detected at the AGC detector (D1061) via the C1061, and enters the base of the AGC amplifier (Q1063) to control the voltage on the AGC line.

The AGC mode is selected by the receiver mode or AGC switch on the front panel using the delay control circuit (Q1064–Q1066). The MDAT signal from the CPU (LOGIC board; IC101, pin 21) is applied to the shift resistor (IC1601, pin 2) to produce the AGSS and the AGFS signals. The AGSS signal is applied to the Q1064, the AGFS signal is applied to the Q1065, the AGRS signal from the CPU (LOGIC unit; IC101, pin 80) is applied to the Q1066 to control the delay control circuit.

The AGRS signal resets the AGC circuit when IC-R75 is working the memory scanning.

When the AGC switch is selected "OFF", the Q1061 do not supply the voltage to the AGC amplifier (Q1063) via the "AGOS" line, determining the time constant to deactivate the AGC circuit.

A portion of the AGC bias voltage is amplified at the S-Meter amplifier circuit (IC1211C, D831), and then applied to the CPU (LOGIC unit; IC101, pin 95) via the "SML" line. Thus, the CPU controls S-Meter display.

### 3-1-13 SQUELCH CIRCUIT (MAIN AND LOGIC UNIT)

The "SML" signal is applied to the CPU (LOGIC unit; IC101, pin 91) from the meter amplifier circuit (IC1211C, D831). The CPU compares "SML" signal with the level of SQL volume on the VR BOARD to control the "SQL" signal.

The CPU is output the "SQLS" signal from pin 81, and then applied to the AF selector circuit (MAIN unit; IC1201, pin 6) which has also the squelch gate circuit.

## 3-2 PLL CIRCUITS

### 3-2-1 GENERAL DESCRIPTION

The PLL unit generates a 1st LO signal (69.0415–129.0115 MHz variable), 2nd LO signal (60 MHz), 3rd LO signal (9.4665 MHz) and BFO signal (455 kHz) used in the MAIN unit.

The IC-R75 uses a DDS (Direct Digital synthesizer) system. The DDS system provides rapid lockup time and high quality frequency oscillation.

### 3-2-2 REFERENCE OSCILLATOR CIRCUIT (PLL CIRCUIT)

The 30 MHz reference oscillator circuit consists of X1 and Q1. The 30 MHz reference frequency is oscillated to produce all of the LO signals.

### 3-2-3 1ST LO CIRCUIT (PLL AND MAIN UNIT)

The 30 MHz reference frequency is applied to the DDS-IC (PLL unit; IC21, pin 40) to oscillate the 1st LO signal. The reference frequency is compared to the DDS output signal (PLL unit; IC21, pin 46) to oscillate the PLL lock voltage. The PLL lock voltage controls the oscillate frequency of the VCO1 and VCO2 circuit.

The oscillated signal at the VCO1 and VCO2 circuit is amplified at the LO-amplifier (PLL unit; Q91), and passes through the low-pass filter (PLL unit; Q92, D91, D92, L91, L93, C96–C100, C102, C103) to suppress high harmonic components. The low-pass filter controls the cut-off frequency of less than 29.999 MHz and more than 30.000 MHz by switching C102 and C103 "ON" and "OFF" respectively.

The filtered signal is applied to the LO-amplifier (MAIN unit; Q411), and is then applied to the 1st mixer circuit (MAIN unit; Q441, Q442) via the low-pass filter (MAIN unit; L421, L422, C422–C425).

The reference frequency from the LO-amplifier (PLL unit; Q91) is also divided by 4 at IC22, and is amplified at the IC23. The signal is applied to the DDS-IC (PLL unit; IC21, pin 88) for the clock signal.

### 3-2-4 2ND LO CIRCUIT (PLL AND MAIN UNIT)

The 30 MHz reference frequency from the Q1 and X1 on the PLL unit is multiplied by 2 at Q2 on the PLL unit. The 60 MHz 2nd LO signal is obtained at the L4 and L5 on the MAIN unit, and is then applied to the 2nd mixer circuit (MAIN unit; D491) via the 3dB attenuator (MAIN UNIT; R491–R493).

### 3-2-5 3RD LO CIRCUIT (PLL AND MAIN UNIT)

The 30 MHz reference frequency is oscillated at the Q1 and X1 on the PLL unit, and is then amplified at the Q151 on the PLL unit. The amplified signal is applied to the 10 bits DDS-IC (PLL unit; IC151, pin 7) for the clock signal to produce the 9.4665 MHz 3rd LO signal. The 3rd LO signal is applied to the D/A converter circuit, and passes through the low-pass filter (PLL unit; L151, L152, C152–C157) to suppress spurious components. The filtered 9.4665 MHz 3rd LO signal is applied to the 3rd mixer circuit (MAIN unit; IC811, pin 10)

### 3-2-6 BFO CIRCUIT (PLL AND MAIN UNIT)

The 30 MHz reference frequency is amplified at the Q201 on the PLL unit, and is applied to the 10 bits DDS-IC (PLL unit; IC201, pin 7) for the clock signal to produce the 455 kHz BFO signal. The BFO signal is applied to the D/A converter circuit, and passes through the low-pass filter (PLL unit, L201, L202, C202–C207) to suppress spurious components. The filtered 455 kHz BFO signal is applied to the BFO mixer circuit (MAIN unit; IC1101, pin 10).

### 3-2-7 VCO CIRCUIT

The VCO circuit consists of the VCO1 circuit (PLL unit; Q71, Q72, D71) and VCO2 circuit (PLL unit; Q81, Q82, D81). The VCO1 controls less than displayed frequency of 29.999 MHz to use the PLL lock voltage from the DDS-IC. The VCO2 controls more than displayed frequency of 30.000 MHz to use the PLL lock voltage from the DDS-IC.

## 3-3 LOGIC CIRCUITS

The LOGIC circuit consists of the CPU, the reset circuit, backup battery circuit, and so on.

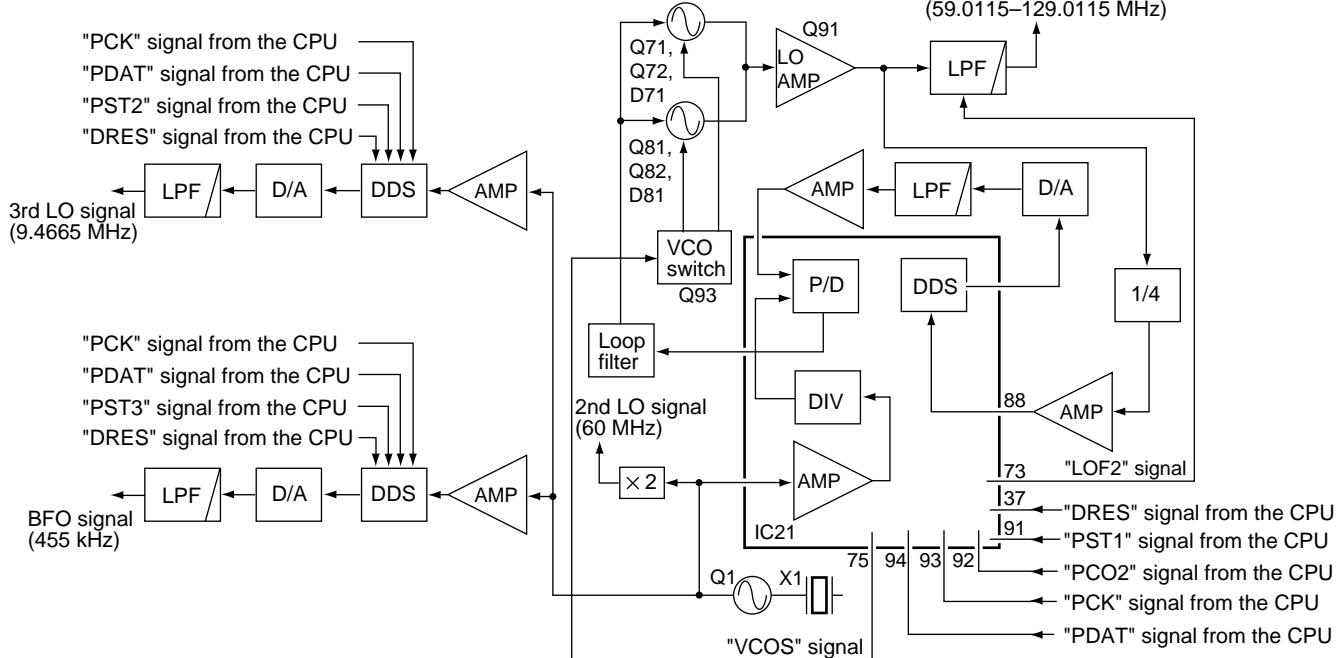
### 3-3-1 CPU (LOGIC UNIT)

The CPU (IC101) contains 8-bit one chip CPU. The CPU controls the operating frequency, mode, function, display, panel switches, panel volumes.

The panel switches are connected the CPU input port to the function of the panel switch or are connected some functions of panel switches to the A/D converter input port in the CPU.

The CI-V signal which is used for communicate to the personal computer is controlled by the level control circuit (IC401A, IC401B, Q401 and so on).

### • PLL circuit



The CPU has the clock function. Thus, the CPU and the clock function have the crystal separately. The CPU has the 9.8304 MHz crystal (X112) for the CPU clock, and then the oscillated 9.8304 MHz signal is applied to the IC101, pin 7 and 8. The clock function has the 32.768 kHz crystal (X111). The oscillated 32.768 kHz signal is applied to the CPU (IC101, pin 4 and 5).

When the power is "OFF", the EEPROM (IC231) is used for keep on saving the data of memory channels, and so on.

### 3-3-2 RESET CIRCUIT (LOGIC UNIT)

The reset circuit consists of Q391, D381, D382, D393, IC391 and IC392. When IC-R75 is supplied 13.8 V to connect the AC adapter, the "HV" signal is applied to the IC391, pin 2. The signal which is output from the IC391, pin 1 is applied to the IC392, pin 1. The signal is applied to the Q391, and is then output to the CPU (IC101, pin 9) as "CRES" reset signal.

A portion of the output signal from the IC392 is input to the CPU (IC101, pin 82) as "BKUP" signal to backup the clock data.

### 3-3-3 BACKUP SWITCH CIRCUIT (LOGIC UNIT)

IC-R75 has a backup switch circuit (Q511 and Q512). When IC-R75 is supplied to 13.8 V to connect the AC adapter, the "H5V" signal is applied to Q512, pin 4, and then Q511 is OFF. When the AC adapter is disconnected, the "BATT" signal from the battery (MAIN unit; BT1521) is applied to the Q511, and then Q512 is OFF.

The output signal is applied to the CPU (IC101, pin 31) as "B5V" signal to keep on working the clock function.

The backup battery is not used while the AC adapter is connected.

## 3-4 POWER SUPPLY CIRCUITS

### 3-4-1 VOLTAGE LINES (MAIN UNIT)

Line	Description
HVR	The voltage from the connected DC power supply.
H5V	Common 5 V converted from the "HVR" line by the +5 regulator circuit (IC1361).
14V	Common 14 V converted from the "HVR" line by the regulator circuit (IC1371 and D1371). The output voltage is applied to the pre-amplifier (Q381 and Q382) via the PRE1 regulator circuit (Q383) and the IF-amplifier (Q471) via the R14V regulator circuit (Q472).
R8V	Receive 8 V converted from the "14V" line by the R8 regulator circuit (Q1381, Q1382 and D1381). The output voltage is applied to the IF-amplifier (Q912, Q471), the switch control circuit (Q151), and the driver circuit (IC561 and IC562, pin 9).
8V	Common 8 V converted from the "14V" line by the +8 regulator circuit (IC1391). The output signal is applied to the low-pass filter (IC1211A, pin 4), buffer amplifiers (Q1051 and Q801), the pre-amplifier (IC391) via the REG2 regulator circuit (Q391) and the AM detector circuit (IC2001, pin 25).
5V	Common 5 V converted from the "14V" line by the +5 regulator circuit (IC1401).
-5V	Common -5 V converted from the "14V" line by the -5 V DC-DC convertor circuit (IC1411, D1412 and D1413).

### 3-5 PORT ALLOCATIONS

#### 3-5-1 CPU (LOGIC UNIT; IC101)

Pin number	Port name	Description
1	KEY6	Input port for [0] and [ENT] switch from the 10-key.
9	CRES	Input port for the reset signal. Low : While the reset switch is pushed.
11	PWRK	Input for the [POWER] switch. Low : While [POWER] switch is pushed.
12	DUD	Input port for the UP signal from the [MAIN DIAL].
14	DAST	Outputs strobe signals for the D/A converter (LOGIC unit; IC351).
15	RSTB	Outputs strobe signals for the shift register (MAIN unit; IC551, IC552).
16	ISTB	Outputs strobe signals for the shift register (MAIN unit; IC1602).
17	ASTB	Outputs strobe signals for the shift register (MAIN unit; IC1601).
18	ECS	Outputs ECS signals for the EEPROM (LOGIC unit; IC231).
19	MCK	Outputs clock signal to the EEPROM and shift registers.
21	MDAT	Outputs data signals to the EEPROM, shift registers, etc.
22	PCK	Outputs clock signals to the PLL IC (PLL unit; IC21) and the DDS IC (PLL unit; IC151, IC201).
23	PST1	Outputs strobe signals for the PLL IC.
24	PDAT	Outputs data signals to the PLL IC and the DDS IC.
25	PST2	Outputs strobe signals for the DDS IC (IC151).
26	PST3	Outputs strobe signals for the DDS IC (IC201).
36	SSBK	Input port for the [SSB] switch.
37	CWK	Input port for the [CW] switch.
38	AMK	Input port for the [AM] switch.
39	FMK	Input port for the [FM] switch.
40	FILK	Input port for the [FIL] switch.
41	TSK	Input port for the [TS] switch.
42	PREK	Input port for the [P.AMP] switch.
43	ATTK	Input port for the [ATT] switch.
44	NRK	Input port for the [NR] switch.
45	ANFK	Input port for the [ANF] switch.
46	NBK	Input port for the [NB] switch.
47	AGCK	Input port for the [AGC] switch.
48	VMK	Input port for the [V/M] switch.

Pin number	Port name	Description
49	MWK	Input port for the [MW] switch.
50	CLRK	Input port for the [CLR] switch.
51	SELK	Input port for the [SEL] switch.
52	SCAK	Input port for the [SCAN] switch.
53	UPK	Input port for the [UP] switch.
54	DNK	Input port for the [DN] switch.
55	LOCK	Input port for the [LOCK] switch.
56	SETK	Input port for the [SET] switch.
57	CLKK	Input port for the [CLOCK] switch.
63	DRES	Outputs reset signal to the PLL IC and DDS IC. Low: PLL IC and DDS IC is reset.
77	PWRS	Outputs control signal for the regulator circuit (MAIN unit; IC1371 and D1371).
78	BEEP	Outputs beep audio signals.
79	RXS	Outputs control signal for the R8 regulator circuit (MAIN unit; Q1381, Q1382, D1381).
80	AGRS	<ul style="list-style-type: none"> <li>Outputs AGC reset signal to the AGC delay control circuit (MAIN unit; Q1066).</li> <li>Outputs control signal for the AGC delay control circuit (MAIN unit; Q1061, Q1064–Q1066).</li> </ul>
81	SQLS	Outputs squelch control signal to the AF selector circuit (MAIN unit; IC1201).
82	BKUP	Input port for the BKUP signal from the reset circuit (LOGIC unit; IC391).
83	DCK	Input port for the UP signal from the [MAIN DIAL].
84	RECS	Outputs control signal for the remote recording driver.
90	AFGL	Input port for the AF gain signal from the [AF] volume on the front panel.
91	RFGL	Input port for the SQL/RF gain signal from the [SQL/RF] volume on the front panel.
92	PB1L	Input port for the PBT1 signal from the [TWIN PBT] volume on the front panel.
93	PB2L	Input port for the PBT2 signal from the [TWIN PBT] volume on the front panel.
94	FMNL	Input port for the FM noise squelch signal from the FM detector circuit (MAIN unit; IC1001 and X1001).

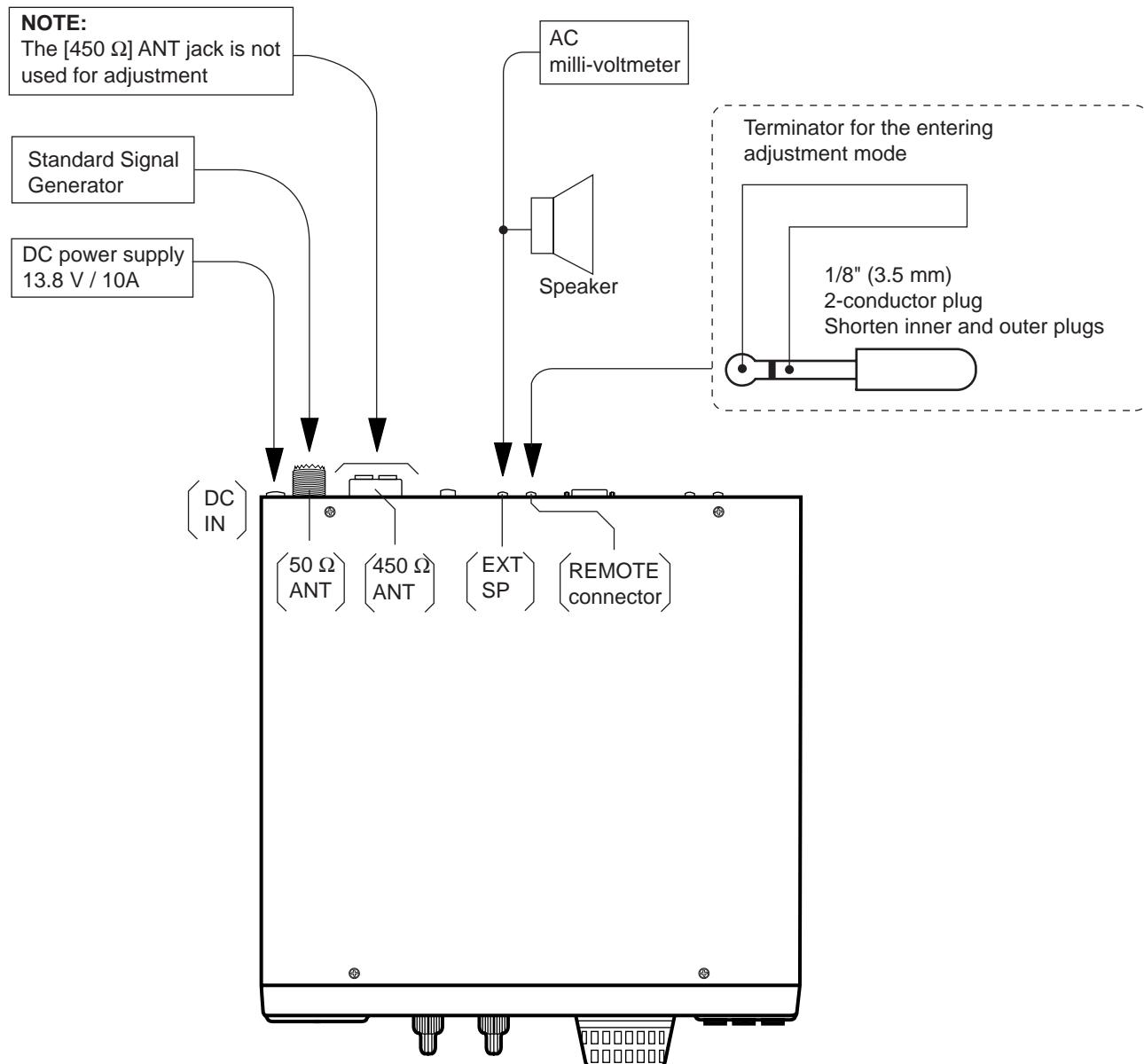
## SECTION 4 ADJUSTMENT PROCEDURES

### 4-1 PREPARATION

#### ■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 13.8 V DC Current capacity : 2 A or more	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
Frequency counter	Frequency range : 0.1–60 MHz	AC millivoltmeter	Measuring range : 10 mV–10 V
	Frequency accuracy : $\pm 1$ ppm or better	External speaker	Input impedance : 8 $\Omega$ Capacity : 4 W or more
	Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 0.1–300 MHz Output level : 0.1 $\mu$ V–32 mV (−127 to −17 dBm)
Audio generator	Frequency range : 0.1–60 Hz Measuring range : 0.01–10 mV		
DC Voltmeter	Input impedance : 50 k $\Omega$ /V DC or better		

#### ■ CONNECTION

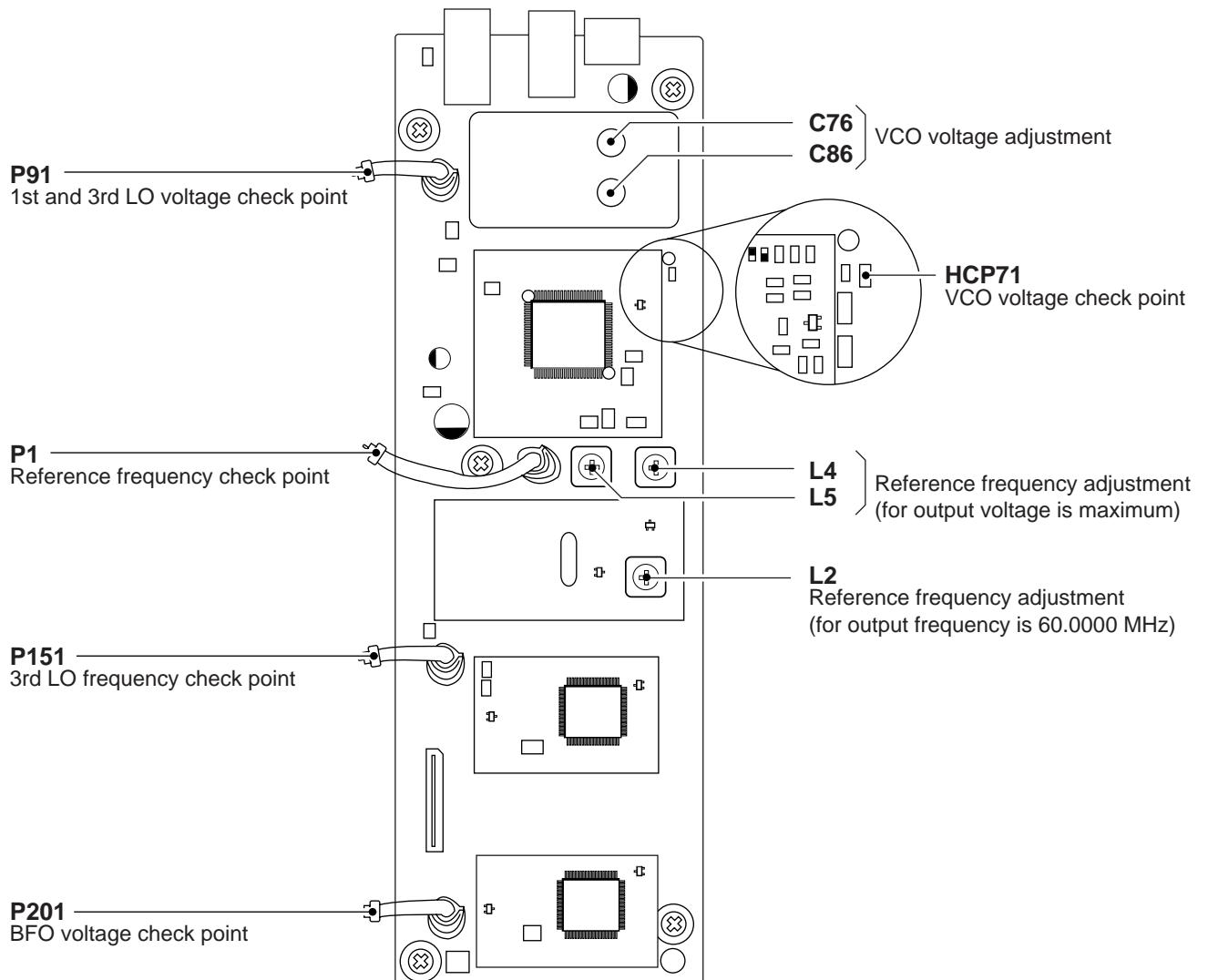


## 4-2 PLL ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
			UNIT	LOCATION		UNIT	ADJUST
REFERENCE FREQUENCY	1	• Displayed frequency : 29.99999 MHz • Mode : USB	PLL	Connect the frequency counter to P1.	60.00000 MHz	PLL	L2
	2			Connect the RF voltmeter to P1.	Maximum voltage		L4, L5
VCO VOLTAGE	1	• Displayed frequency : 29.99999 MHz • Mode : USB	PLL	Connect the DC voltmeter to HCP71.	4.0 V	PLL	C86
	2	• Displayed frequency : 0.03000 MHz • Mode : USB			More than 0.8 V		Verify
	3	• Displayed frequency : 60.00000 MHz • Mode : USB			4.0 V	PLL	C76
	4	• Displayed frequency : 30.00000 MHz • Mode: USB			More than 0.8 V		Verify
1ST LO VOLTAGE	1	• Displayed frequency : 30–60.00000 MHz • Mode : USB	PLL	Connect the RF voltmeter to P91.	More than 0.18 V		Verify
3RD LO VOLTAGE	1	• Displayed frequency : 30–60.00000 MHz • Mode : USB	PLL	Connect the RF voltmeter to P91.	More than 0.022 V		Verify
3RD LO FREQUENCY	1	• Displayed frequency : 9.4615 MHz • Mode : FM	PLL	Connect the frequency counter to P151.	9.4614–9.4616 MHz		Verify
BFO VOLTAGE	1	• Displayed frequency : 14.100000 MHz • Mode : USB	PLL	Connect the RF voltmeter to P201.	More than 0.022 V		Verity
	2	• Displayed frequency : 14.100000 MHz • Mode : AM			Less than 280 $\mu$ V		

\*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.

• PLL UNIT

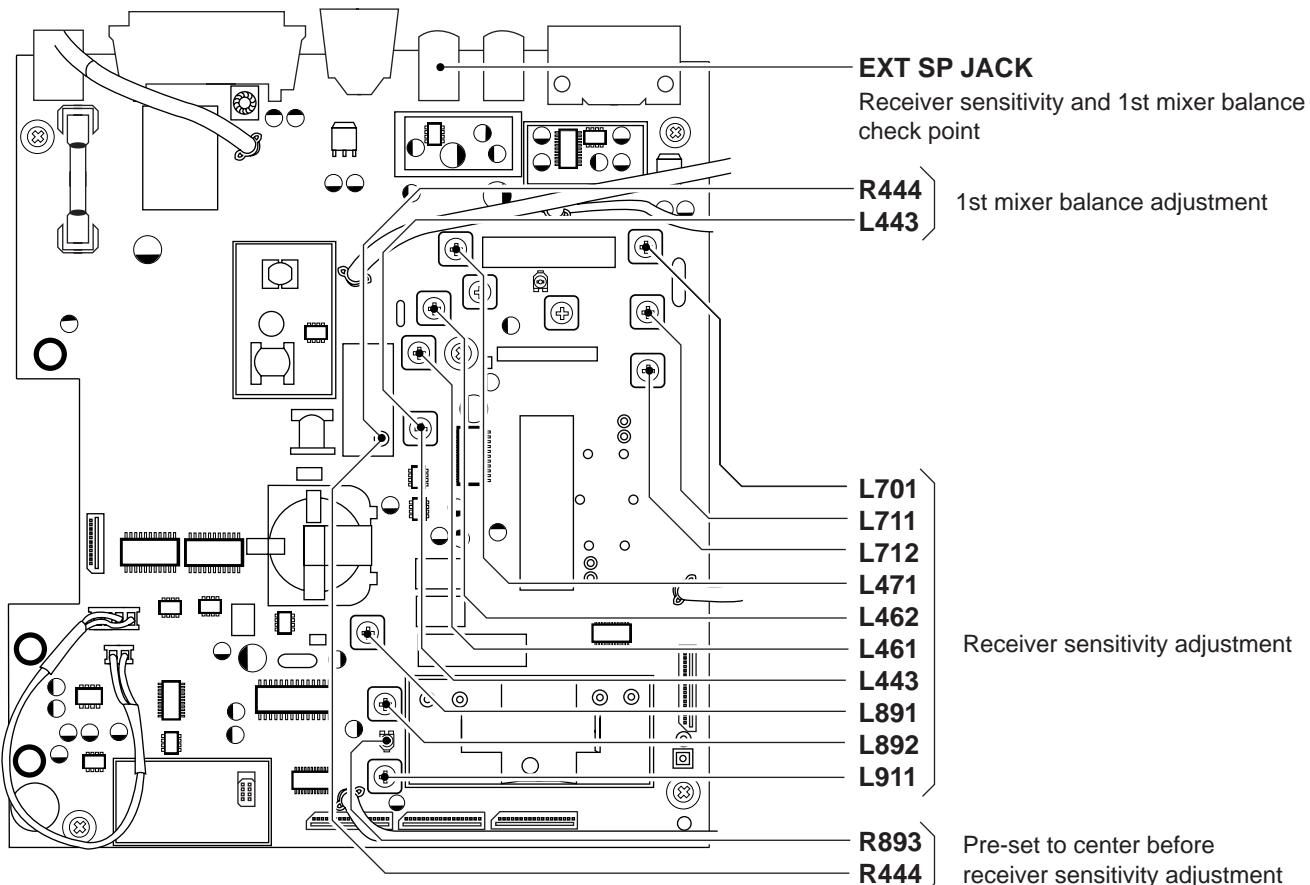


### 4-3 RECEIVER ADJUSTMENTS

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT		
		UNIT	LOCATION		UNIT	ADJUST	
RECEIVER SENSITIVITY	1	• Displayed frequency : 14.10000 MHz • Mode : USB • PREAMP1 : ON • ANT select : ANT1 • AGC : FAST • NOISE BLANKER : OFF • RF/SQL : CENTER • PBT1/PBT2 : CENTER • IF FILTER1 : 2.4 kHz • IF FILTER2 : 2.4 kHz	Rear Panel	Connect the AC milli-volt meter to the [EXT SP] jack with an 8 Ω load.	Pre-set to center	MAIN	R444 R898
	2	• Connect an SSG to the antenna connector1 and set as: Frequency : 14.10150 MHz Level : 22 μV* (-13 dBμ) Modulation : OFF • Receiving			Maximum output level	MAIN	L443, L461, L462, L471, L701, L711, L712, L891, L892, L911
1ST MIXER BALANCE	1	• Displayed frequency : 0.10000 MHz • PREAMP1 : OFF • set an SSG level as : OFF • Receiving	Rear panel	Connect an oscilloscope to the [EXT SP] jack with 8 Ω load.	Minimum noise level	MAIN	L443, R444

\*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.

#### • MAIN UNIT

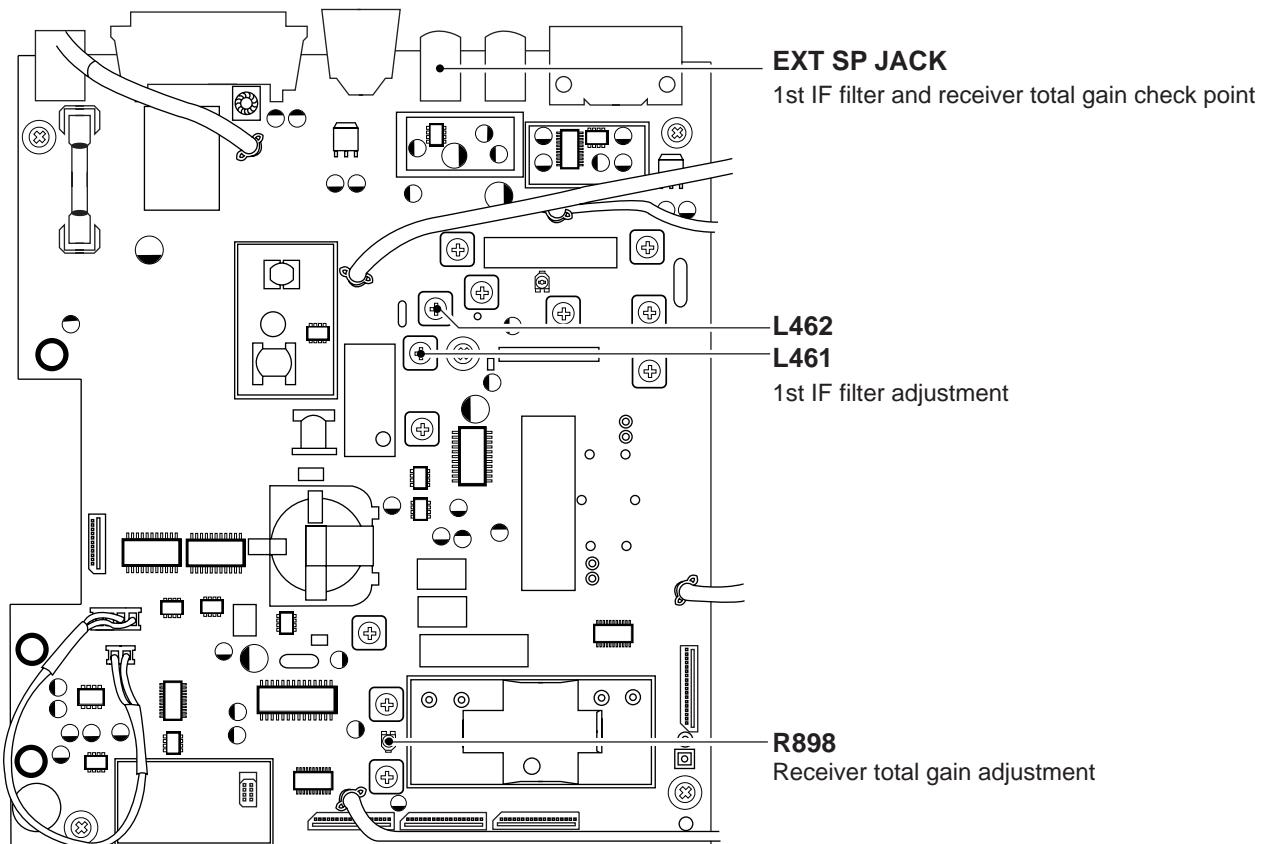


## RECEIVER ADJUSTMENTS (continued)

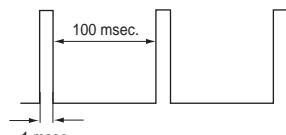
ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
		UNIT	LOCATION		UNIT	ADJUST
1ST IF FILTER	1	• Displayed frequency : 14.10000 MHz • Mode : FM • PREAMP1 : ON • IF FILTER1 : 15 kHz • IF FILTER2 : 6 kHz • set an SSG as Frequency : 14.10000 MHz Level : 0.32 $\mu$ V* (-10 dB $\mu$ ) Deviation : $\pm$ 3.5 kHz Modulation : 1 kHz • Receiving	Rear panel	Connect the AC milli-volt meter to the [EXT SP] jack with an 8 $\Omega$ load.	Maximum output level	MAIN L461, L462
RECEIVER TOTAL GAIN	1	• Displayed frequency : 14.10000 MHz • Mode : USB • PREAMP1 : OFF • IF FILTER1 : 2.4 kHz • IF FILTER2 : 2.4 kHz • Set an SSG as Frequency : 14.10150 MHz Level : 500 $\mu$ V* (54 dB $\mu$ ) Modulation : OFF	Rear panel	Connect the AC milli-volt meter to the [EXT SP] jack with an 8 $\Omega$ load.	0 dB (1.0 V)	Front panel [AF GAIN] control
	2	• Set an SSG level as : OFF • Receiving			-30 dB (10 mV)	MAIN R898

\*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.

### • MAIN UNIT

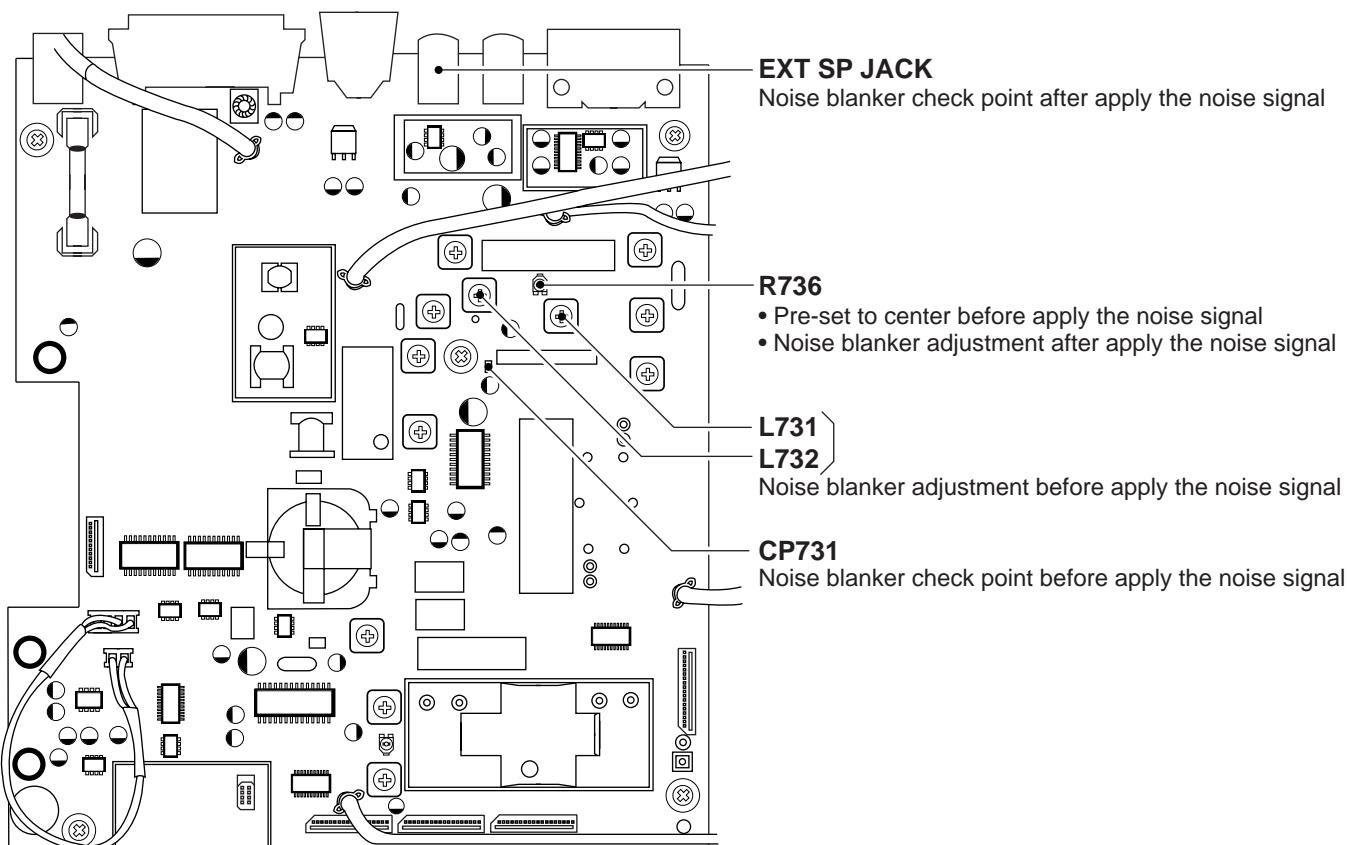


## RECEIVER ADJUSTMENTS (CONTINUED)

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT		
		UNIT	LOCATION		UNIT	ADJUST	
NOISE BLANKER	1	• Displayed frequency : 14.10000 MHz • Mode : USB • Noise Blanker : OFF • PREAMP1. : ON • Set an SSG as Frequency : 14.10000 MHz Level : 18 $\mu$ V* (25 dB $\mu$ ) Modulation : OFF	MAIN	Connect the oscilloscope to the check point CP731.	Pre-set to center Minimum voltage	MAIN	R736 L731, L732
	2	• Apply the following signal to the [ANT1] connector 	Rear Panel	Connect the oscilloscope to the [EXT SP] jack with an 8 $\Omega$ load.	Noise is blanked when the [NB] switch is ON.	MAIN	R736

\*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.

### • MAIN UNIT



#### 4-4 SET MODE ADJUSTMENT

ADJUSTMENT	ADJUSTMENT CONDITION	DISPLAY	OPERATION
ENTERING ADJUSTMENT SET MODE	<ul style="list-style-type: none"> <li>• Turn power OFF</li> <li>• Connect a terminator to the [REMOTE] connector on the rear panel.</li> <li>• While pushing “SET[ANT]” and “CLOCK” keys, and turn power ON.</li> </ul>	<b>PBT SET</b>	<ul style="list-style-type: none"> <li>• When success entering adjustment set mode, shown “PBT SET” on the display.</li> <li>• Then advance to the following setting, or push “UP” key to scroll the display.</li> </ul>
PBT VOLUME	<p>1</p> <ul style="list-style-type: none"> <li>• Connect an SSG to the antenna connector1 and set as:</li> <li>Frequency : 14.15150 MHz</li> <li>Level : 50 mV* (-13 dBm)</li> <li>Modulation : OFF</li> <li>• Preset both the inner and outer “TWIN PBT” controls to 12 o'clock position.</li> <li>• Receiving</li> </ul>	<b>GOOD</b>	<ul style="list-style-type: none"> <li>• Push “SET[ANT]” key to set the PBT level.</li> <li>• When the PBT level is true, shown “GOOD” on the display.</li> </ul>
S-METER	<p>1</p> <ul style="list-style-type: none"> <li>• Set an SSG level as : OFF</li> </ul>	<b>50 LV</b>	<ul style="list-style-type: none"> <li>• When S0 level of S-meter adjustment mode entering, displayed “S0 LV”.</li> <li>• Push the “SET[ANT]” key to set the S0 level.</li> </ul>
	<p>2</p> <ul style="list-style-type: none"> <li>• Set an SSG level as : 35 µV* (31 dBµ)</li> </ul>	<b>59 LV</b>	<ul style="list-style-type: none"> <li>• When S9 level of S-meter adjustment mode entering, displayed “S9 LV”.</li> <li>• Push the “SET[ANT]” key to set the S9 level.</li> </ul>
	<p>3</p> <ul style="list-style-type: none"> <li>• Set an SSG level as : 28 mV* (89 dBµ)</li> </ul>	<b>+60 LV</b>	<ul style="list-style-type: none"> <li>• When +60 dB level of S-meter adjustment mode entering, displayed “+60 LV”.</li> <li>• Push the “SET[ANT]” key to set the 60 dB level.</li> </ul>
	<p>4</p>	<b>END</b>	<ul style="list-style-type: none"> <li>• When the S-meter adjustment is end, displayed “END”.</li> </ul>
FILTER CALIBRATION	<p>1</p> <ul style="list-style-type: none"> <li>• Set an SSG level as : 10 µV* (20 dBµ)</li> </ul> <p>2</p> <ul style="list-style-type: none"> <li>• Turn power OFF to exit the adjustment set mode.</li> </ul>	<b>FIL CAL</b>	<ul style="list-style-type: none"> <li>• When filter calibration adjustment mode entering, displayed “FIL CAL”.</li> <li>• Push the “SET[ANT]” key to set the filter calibration.</li> <li>• Emit to the beep audio.</li> </ul>

\*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.

















[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	
J884	6450001560	CONNECTOR	PD-72
J1081	6510007020	CONNECTOR	TMP-J01X-V6
J1221	6510018970	S.CONNECTOR	B4B-PH-SM3-TB
J1231	6510019970	S.CONNECTOR	52808-1090
J1271	6510019190	S.CONNECTOR	52365-0891
J1311	6450001800	CONNECT	JPJ1044-01-010
J1321	6450000140	CONNECTOR	HSJ0807-01-010
J1351	6450001700	CONNECTOR	HEC0740-010010
J1501	6510019980	S.CONNECTOR	52808-1690
J1521	6510019980	S.CONNECTOR	52808-1690
J1522	6510008370	CONNECTOR	BBH-1
J1541	6510019980	S.CONNECTOR	52808-1690
J1561	6510019980	S.CONNECTOR	52808-1690
J1701	6450000140	CONNECTOR	HSJ0807-01-010
J1751	6510021240	CONNECTOR	DELC-J9SAF-23L9
F1351	5210000050	FUSE	FGB 3A
F1352	5220000230	HOLDER	S-N5054 #01
F1353	5220000230	HOLDER	S-N5054 #01
BT1521	3020000110	LITHIUM	CR2032
WS1	8600036540	CABLE	RX2240 P1241*J1241MA
EP1	0910051114	PCB	B 5273D

[PLL UNIT]

REF NO.	ORDER NO.	DESCRIPTION	
L5	6150004250	COIL	LS-471A (C-14922)
L22	6200003170	S.COIL	NL 322522T-330J
L23	6200003180	S.COIL	NL 322522T-390J
L24	6200003180	S.COIL	NL 322522T-390J
L25	6200001830	S.COIL	NL 322522T-100J
L26	6200003190	S.COIL	NL 322522T-470J
L27	6200003190	S.COIL	NL 322522T-470J
L71	6170000230	COIL	LW-25
L72	6190001370	COIL	E544GN-110254
L73	6170000230	COIL	LW-25
L81	6170000230	COIL	LW-25
L82	6190001280	COIL	E544GN-110248
L83	6170000230	COIL	LW-25
L91	6180002960	S.COIL	NL 322522T-R18J-3
L92	6180002980	S.COIL	NL 322522T-056J
L93	6180002970	S.COIL	NL 322522T-068J
L94	6200001830	S.COIL	NL 322522T-100J
L151	6200003130	S.COIL	NL 322522T-120J
L152	6200003140	S.COIL	NL 322522T-150J
L153	6200001830	S.COIL	NL 322522T-100J
L201	6200005490	S.COIL	NL 322522T-331J
L202	6200008640	S.COIL	NL 322522T-391J
L203	6200001830	S.COIL	NL 322522T-100J
L204	6200003640	S.COIL	MLF1608K 100K-T
L205	6200003640	S.COIL	MLF1608K 100K-T

R1	7030003320	S.RESISTOR	ERJ3GEYJ 101 V (100 Ω)
R2	7030003580	S.RESISTOR	ERJ3GEYJ 153 V (15 kΩ)
R3	7030003520	S.RESISTOR	ERJ3GEYJ 472 V (4.7 kΩ)
R4	7030003400	S.RESISTOR	ERJ3GEYJ 471 V (470 Ω)
R5	7030003360	S.RESISTOR	ERJ3GEYJ 221 V (220 Ω)
R6	7030003320	S.RESISTOR	ERJ3GEYJ 101 V (100 Ω)
R7	7030003600	S.RESISTOR	ERJ3GEYJ 223 V (22 kΩ)
R8	7030003560	S.RESISTOR	ERJ3GEYJ 103 V (10 kΩ)
R9	7030003370	S.RESISTOR	ERJ3GEYJ 271 V (270 Ω)
R10	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R11	7030003290	S.RESISTOR	ERJ3GEYJ 560 V (56 Ω)
R12	7030003200	S.RESISTOR	ERJ3GEYJ 100 V (10 Ω)
R21	7030003360	S.RESISTOR	ERJ3GEYJ 221 V (220 Ω)
R22	7030003560	S.RESISTOR	ERJ3GEYJ 103 V (10 kΩ)
R23	7030005400	S.RESISTOR	RR0816P-202-D (2 kΩ)
R24	7030005400	S.RESISTOR	RR0816P-202-D (2 kΩ)
R25	7030005400	S.RESISTOR	RR0816P-202-D (2 kΩ)
R26	7030005400	S.RESISTOR	RR0816P-202-D (2 kΩ)
R27	7030005400	S.RESISTOR	RR0816P-202-D (2 kΩ)
R28	7030005400	S.RESISTOR	RR0816P-202-D (2 kΩ)
R29	7030005400	S.RESISTOR	RR0816P-202-D (2 kΩ)
R30	7030005400	S.RESISTOR	RR0816P-202-D (2 kΩ)
R31	7030005370	S.RESISTOR	RR0816P-202-B (2 kΩ)
R32	7030005370	S.RESISTOR	RR0816P-202-B (2 kΩ)
R33	7030005370	S.RESISTOR	RR0816P-202-B (2 kΩ)
R34	7030005370	S.RESISTOR	RR0816P-202-B (2 kΩ)
R35	7030005370	S.RESISTOR	RR0816P-202-B (2 kΩ)
R36	7030005390	S.RESISTOR	RR0816P-102-D (1 kΩ)
R37	7030005390	S.RESISTOR	RR0816P-102-D (1 kΩ)
R38	7030005390	S.RESISTOR	RR0816P-102-D (1 kΩ)
R39	7030005390	S.RESISTOR	RR0816P-102-D (1 kΩ)
R40	7030005390	S.RESISTOR	RR0816P-102-D (1 kΩ)
R41	7030005390	S.RESISTOR	RR0816P-102-D (1 kΩ)
R42	7030005380	S.RESISTOR	RR0816P-102-B (1 kΩ)
R43	7030005380	S.RESISTOR	RR0816P-102-B (1 kΩ)
R44	7030005380	S.RESISTOR	RR0816P-102-B (1 kΩ)
R45	7030005380	S.RESISTOR	RR0816P-102-B (1 kΩ)
R46	7030005380	S.RESISTOR	RR0816P-102-B (1 kΩ)
R47	7030003400	S.RESISTOR	ERJ3GEYJ 471 V (470 Ω)
R48	7030003720	S.RESISTOR	ERJ3GEYJ 224 V (220 kΩ)
R49	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R50	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R51	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R52	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R53	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R54	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R55	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R71	7030003490	S.RESISTOR	ERJ3GEYJ 272 V (2.7 kΩ)
R72	7030003780	S.RESISTOR	ERJ3GEYJ 684 V (680 kΩ)
R73	7030003260	S.RESISTOR	ERJ3GEYJ 330 V (33 Ω)
R75	7030003390	S.RESISTOR	ERJ3GEYJ 391 V (390 Ω)
R76	7030003250	S.RESISTOR	ERJ3GEYJ 270 V (27 Ω)
R78	7030003370	S.RESISTOR	ERJ3GEYJ 271 V (270 Ω)
R79	7030003580	S.RESISTOR	ERJ3GEYJ 153 V (15 kΩ)
R80	7030003570	S.RESISTOR	ERJ3GEYJ 123 V (12 kΩ)

S.=Surface mount



**[PLL UNIT]**

REF NO.	ORDER NO.	DESCRIPTION	
C99	4030006930	S.CERAMIC	C1608 CH 1H 020C-T-A
C100	4030007080	S.CERAMIC	C1608 CH 1H 390J-T-A
C101	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C102	4030007020	S.CERAMIC	C1608 CH 1H 120J-T-A
C103	4030006970	S.CERAMIC	C1608 CH 1H 060D-T-A
C104	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C105	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C106	4510006220	S.ELECTROLYTIC	ECEV1CA101UP
C107	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C108	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C110	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C111	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C112	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C113	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C114	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C115	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C116	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C117	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C118	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C119	4510004430	S.ELECTROLYTIC	ECEV1CV220WR
C120	4030006850	S.CERAMIC	C1608 JB 1H 471K-T-A
C121	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C122	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C123	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C124	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C125	4030007090	S.CERAMIC	C1608 CH 1H 470J-T-A
C126	4550006250	S.TANTALUM	TEMSVA 1A 106M-8L
C127	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C128	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C151	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C152	4030007040	S.CERAMIC	C1608 CH 1H 180J-T-A
C153	4030006960	S.CERAMIC	C1608 CH 1H 050C-T-A
C154	4030007070	S.CERAMIC	C1608 CH 1H 330J-T-A
C155	4030006930	S.CERAMIC	C1608 CH 1H 020C-T-A
C156	4030007040	S.CERAMIC	C1608 CH 1H 180J-T-A
C157	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C164	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C165	4510004630	S.ELECTROLYTIC	ECEV1CA100SR
C167	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C201	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C202	4030006850	S.CERAMIC	C1608 JB 1H 471K-T-A
C203	4030007120	S.CERAMIC	C1608 CH 1H 820J-T-A
C204	4030009490	S.CERAMIC	C1608 JB 1H 821K-T-A
C205	4030007070	S.CERAMIC	C1608 CH 1H 330J-T-A
C206	4030010040	S.CERAMIC	C1608 JB 1H 561K-T-A
C207	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C214	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C215	4510004630	S.ELECTROLYTIC	ECEV1CA100SR
C217	4030011600	S.CERAMIC	C1608 JB 1C 104KT-N
C305	4510004630	S.ELECTROLYTIC	ECEV1CA100SR
C310	4030007090	S.CERAMIC	C1608 CH 1H 470J-T-A
C311	4030007090	S.CERAMIC	C1608 CH 1H 470J-T-A
C312	4030007090	S.CERAMIC	C1608 CH 1H 470J-T-A
C313	4030007090	S.CERAMIC	C1608 CH 1H 470J-T-A
C314	4030007090	S.CERAMIC	C1608 CH 1H 470J-T-A
C315	4030007090	S.CERAMIC	C1608 CH 1H 470J-T-A
C316	4030007090	S.CERAMIC	C1608 CH 1H 470J-T-A
C317	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C318	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C319	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C320	4030006850	S.CERAMIC	C1608 JB 1H 471K-T-A
C321	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C322	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C323	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C324	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C325	4030007100	S.CERAMIC	C1608 CH 1H 560J-T-A
C326	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C327	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
RL1	6330001320	RELAY	AHY103
J2	6510019980	S.CONNECTOR	52808-1690
J3	6450000140	CONNECTOR	HSJ0807-01-010
J4	6450000140	CONNECTOR	HSJ0807-01-010
W1	7030003860	S.JUMPER	ERJ3GE JPW V
W2	7030003860	S.JUMPER	ERJ3GE JPW V
W18	7030003860	S.JUMPER	ERJ3GE JPW V
W19	7030003860	S.JUMPER	ERJ3GE JPW V

**[PLL UNIT]**

REF NO.	ORDER NO.	DESCRIPTION	
WS1	8970023350	M.OTHER	RX2240 1.5DCOAXIAL (4)/PL
EP1	0910051124	PCB	B 5274D
EP2	6910012350	S.BEAD	MMZ1608Y 102BT
EP3	6910012350	S.BEAD	MMZ1608Y 102BT
EP4	6910012350	S.BEAD	MMZ1608Y 102BT
EP5	6910012350	S.BEAD	MMZ1608Y 102BT
EP6	6910012350	S.BEAD	MMZ1608Y 102BT
EP7	6910012350	S.BEAD	MMZ1608Y 102BT
EP8	6910012350	S.BEAD	MMZ1608Y 102BT

S.=Surface mount

## SECTION 6 MECHANICAL PARTS AND DISASSEMBLY

### [CHASSIS PARTS]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
J1	6510000370	Connector MR-DS	1
W3	8900007000	Cable OPC-684	1
W4	8900007000	Cable OPC-684	1
W5	8900007000	Cable OPC-684	1
W6	8900007000	Cable OPC-684	1
MP1	8010017710	2240 main Chassis	1
MP2	8110006700	2240 U-cover	1
MP3	8110006690	2240 L-cover	1
MP4	8930005790	Collar foot (A)	1
MP5	8930005800	Collar foot (B)	1
MP6	8010001520	Stand (C)	1
MP7	8930002900	Rubbr foot (A)	2
MP8	8930035240	1546 TR-B Clip	1
MP9	8930049600	2240 IC Clip	1
MP10	8810008660	Screw PH BO M3x8 NI-ZU (BT)	4
MP11	8810008660	Screw PH BO M3x8 NI-ZU (BT)	2
MP12	8810008660	Screw PH BO M3x8 NI-ZU (BT)	2
MP13	8810005770	Screw Bih M3x8 ZK	8
MP14	8810005770	Screw Bih M3x8 ZK	2
MP15	8810008660	Screw PH BO M3x8 NI-ZU (BT)	6
MP16	8810008660	Screw PH BO M3x8 NI-ZU (BT)	5
MP17	8810008660	Screw PH BO M3x8 NI-ZU (BT)	2
MP18	8810008660	Screw PH BO M3x8 NI-ZU (BT)	1
MP19	8930037001	1691 Earth plate	1
MP20	8810008660	Screw PH BO M3x8 NI-ZU (BT)	2
MP22	8810009130	Screw PH BO M3x12 NI-ZU (BT)	2
MP23	8410002310	2240 Heatsink	1
MP24	8810008660	Screw PH BO M3x8 NI-ZU (BT)	2
MP25	8930049610	2240 Unit holder	1
MP26	8810003960	Screw M2.6x5	2

### [DISPLAY UNIT]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
DS101	5030001690	LCD HLCF7395-012400	1
EP2	8930049630	LCD contact SRCN-2240-SP-N-W	1
MP1	8210016060	2240 Reflector	1
MP2	8930048880	2240 LCD Holder	1
MP3	8930049380	2240 LCD Filter	1

### [MAIN UNIT]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
MP382	8510005990	724 Shield case cover	1
MP442	8510005160	602 Shield case cover	1

### [PLL UNIT]

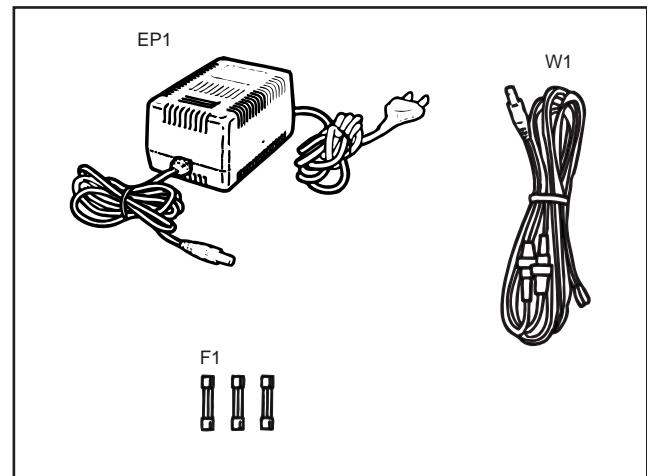
REF. NO.	ODER NO.	DESCRIPTION	QTY.
MP3	8510010770	1876 DDS cover	1
MP9	8510005990	724 Shield case cover	1
MP12	8510005990	724 Shield case cover	1

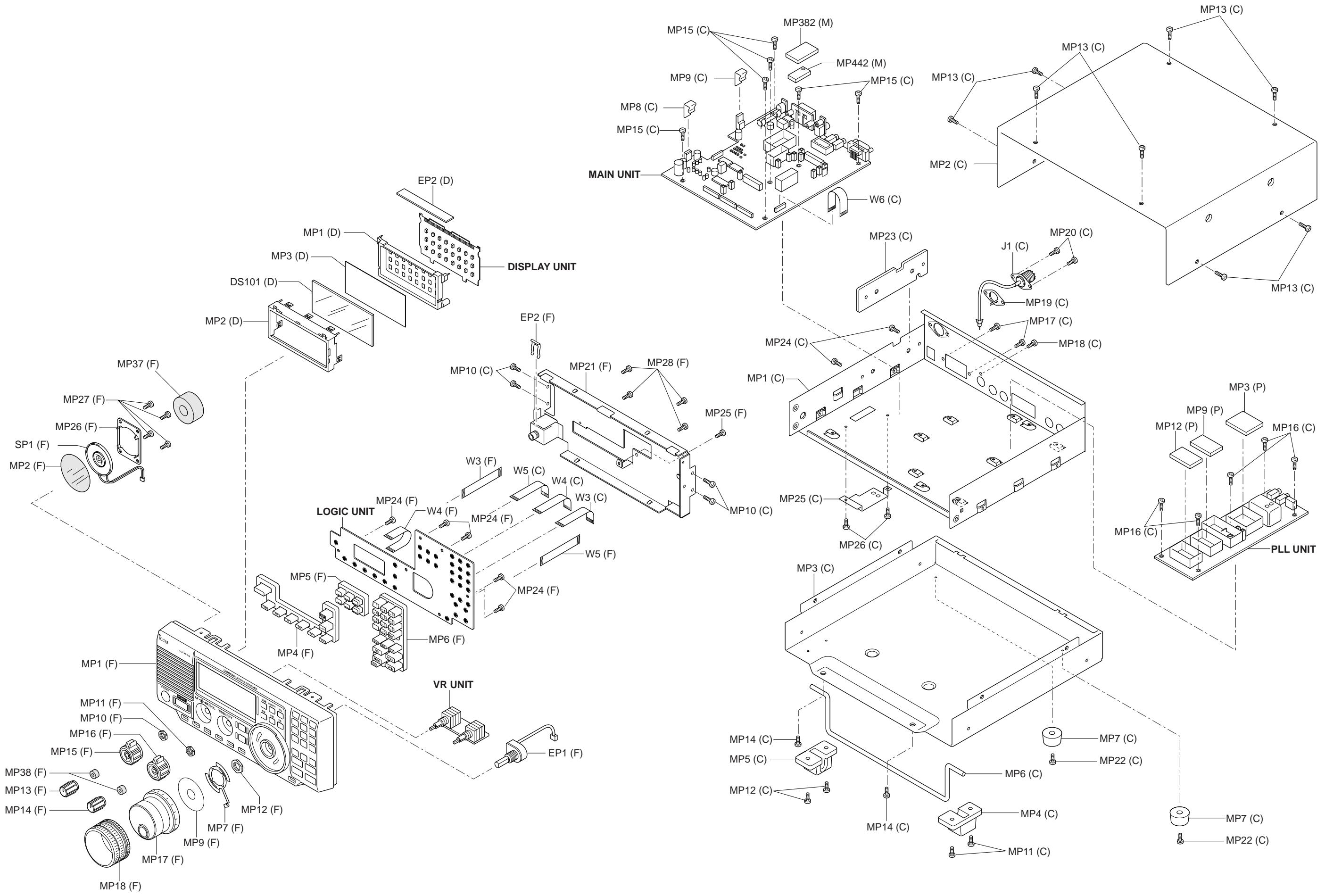
### [ACCESSORIES]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
F1	Optional product	Fuse FGB 3A [USA], [EUR], [OTH]	1
	Optional product	Fuse FGB 3A [UK], [SEA]	3
W1	Optional product	Cable OPC-869 [UK], [SEA]	1
EP1	Optional product	Charger AD-55A [USA]	1
	Optional product	Charger AD-55 [EUR], [OTH]	1
	Optional product	Charger AD-55V [AUS]	1

### [FRONT UNIT]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
SP1	2510000670	VS-50-0827	1
W3	8900008940	Cable OPC-886	1
W4	8900008930	Cable OPC-885	1
W5	8900007000	Cable OPC-684	1
EP1	6910012480	RMS20-250-201-1R	1
EP2	6450001230	Snap plate HLJ0999-01-480	1
MP1	8210016030	2240 Front cover	1
MP2	8930001770	SP net	1
MP4	8930048740	2240 9-Key	1
MP5	8930048730	2240 6-Key	1
MP6	8930048750	2240 20-Key	1
MP7	8930048710	2240 Brake plate	1
MP9	8930049370	2240 Brake sheet	1
MP10	8830001010	Screw Hex nut (A)	1
MP11	8830001010	Screw Hex nut (A)	1
MP12	8830001410	1897 Nut	1
MP13	8610010420	Knob N-261	1
MP14	8610010420	Knob N-261	1
MP15	8610010710	Knob N-272	1
MP16	8610010710	Knob N-272	1
MP17	8610009160	Knob N-213 Base	1
MP18	8610009170	Knob N-213 Cover	1
MP21	8010017770	2240 F-Chassis	1
MP24	8810008660	Screw PH BO M3x8 NI-ZU (BT)	5
MP25	8810008660	Screw PH BO M3x8 NI-ZU (BT)	1
MP26	8930048890	2240 SP holder	1
MP27	8810008660	Screw PH BO M3x8 NI-ZU (BT)	4
MP28	8810008660	Screw PH BO M3x8 NI-ZU (BT)	4
MP37	8930049870	2240 SP sponge	1
MP38	8930049840	Knob sheet (B)	2

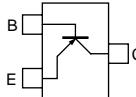
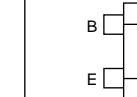
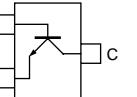
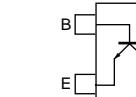
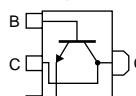
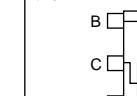
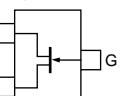
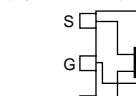
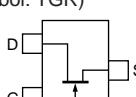
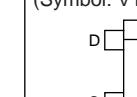
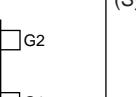
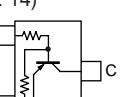
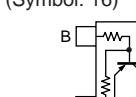
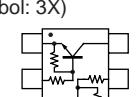
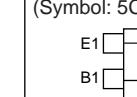




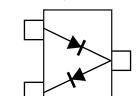
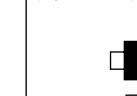
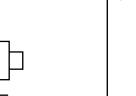
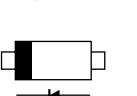
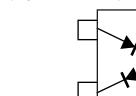
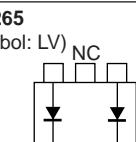
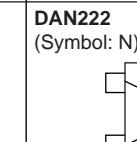
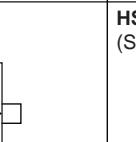
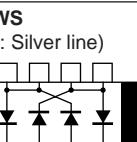
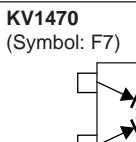
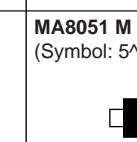
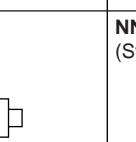
**UNIT abbreviation** (C): CHASSIS PARTS, (P): PLL UNIT, (M): MAIN UNIT, (F): FRONT UNIT, (D): DISPLAY UNIT

## SECTION 7 SEMI-CONDUCTOR INFORMATION

● TRANSISTOR AND FET'S

<b>2SA1576 R</b> (Symbol: FR) 	<b>2SC4081 R</b> (Symbol: BR) 	<b>2SC4116 BL</b> (Symbol: LL) 	<b>2SC4117 BL</b> (Symbol: CL) 	<b>2SC4405 3</b> (Symbol: OY3) 
<b>2SC4673 D</b> (Symbol: CO) 	<b>2SD1664 Q</b> (Symbol: DA) 	<b>2SK1740</b> (Symbol: IJ) 	<b>2SK2171 4</b> (Symbol: KM) 	<b>2SK508 K52</b> (Symbol: K52) 
<b>2SK882 GR</b> (Symbol: TGR) 	<b>3SK131 MAS</b> (Symbol: V11) 	<b>DTA114 EU</b> (Symbol: 14) 	<b>DTA144 EU</b> (Symbol: 16) 	<b>DTC114 EU</b> (Symbol: 14) 
<b>XP4311</b> (Symbol: 3X) 	<b>XP4601</b> (Symbol: 5C) 			

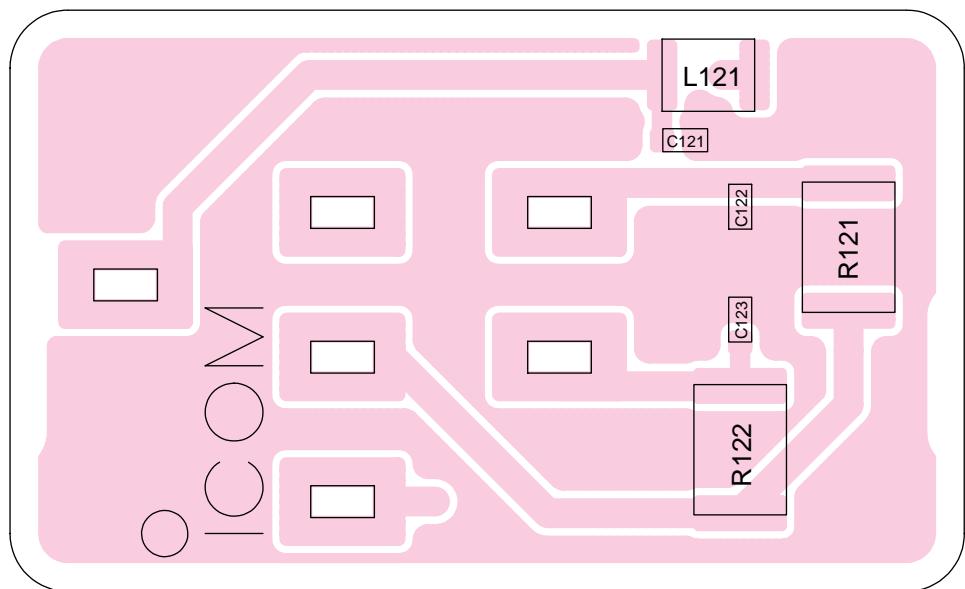
● DIODES

<b>1SS302</b> (Symbol: C3) 	<b>1SS355</b> (Symbol: A) 	<b>1SS373</b> (Symbol: S4) 	<b>1SS375</b> (Symbol: FH) 	<b>1SV263</b> (Symbol: JV) 
<b>1SV265</b> (Symbol: LV) 	<b>DAN222</b> (Symbol: N) 	<b>HSB88WS</b> (Symbol: Silver line) 	<b>KV1470</b> (Symbol: F7) 	<b>MA729</b> (Symbol: 2B) 
<b>MA77</b> (Symbol: 4B) 	<b>MA8051 M</b> (Symbol: 5^1) 	<b>NNCD6.2G</b> (Symbol: 6.2G) 		

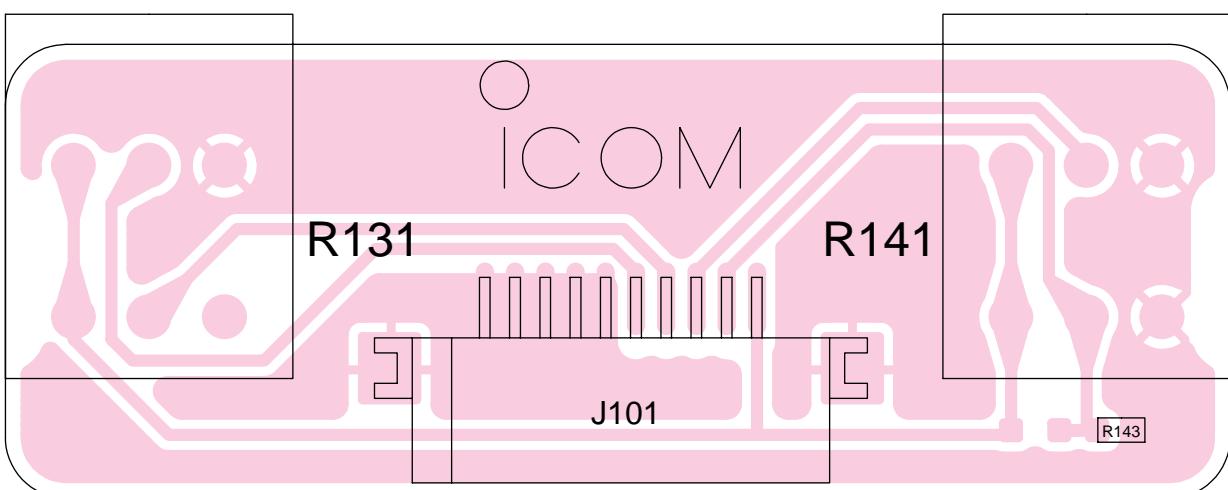
## SECTION 8     BOARD LAYOUTS

### 8-1 PHONE AND VR BOARDS

- PHONE BOARD  
TOP VIEW

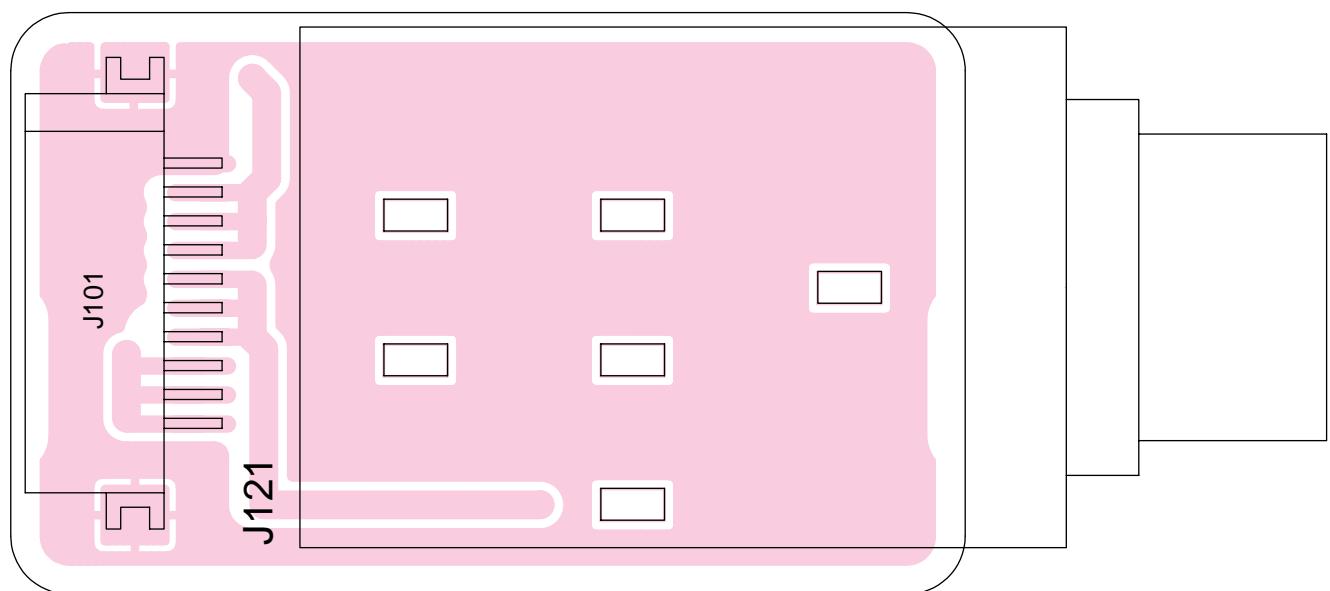


- VR BOARD



J101  
to LOGIC board J451

• PHONE BOARD  
BOTTOM VIEW

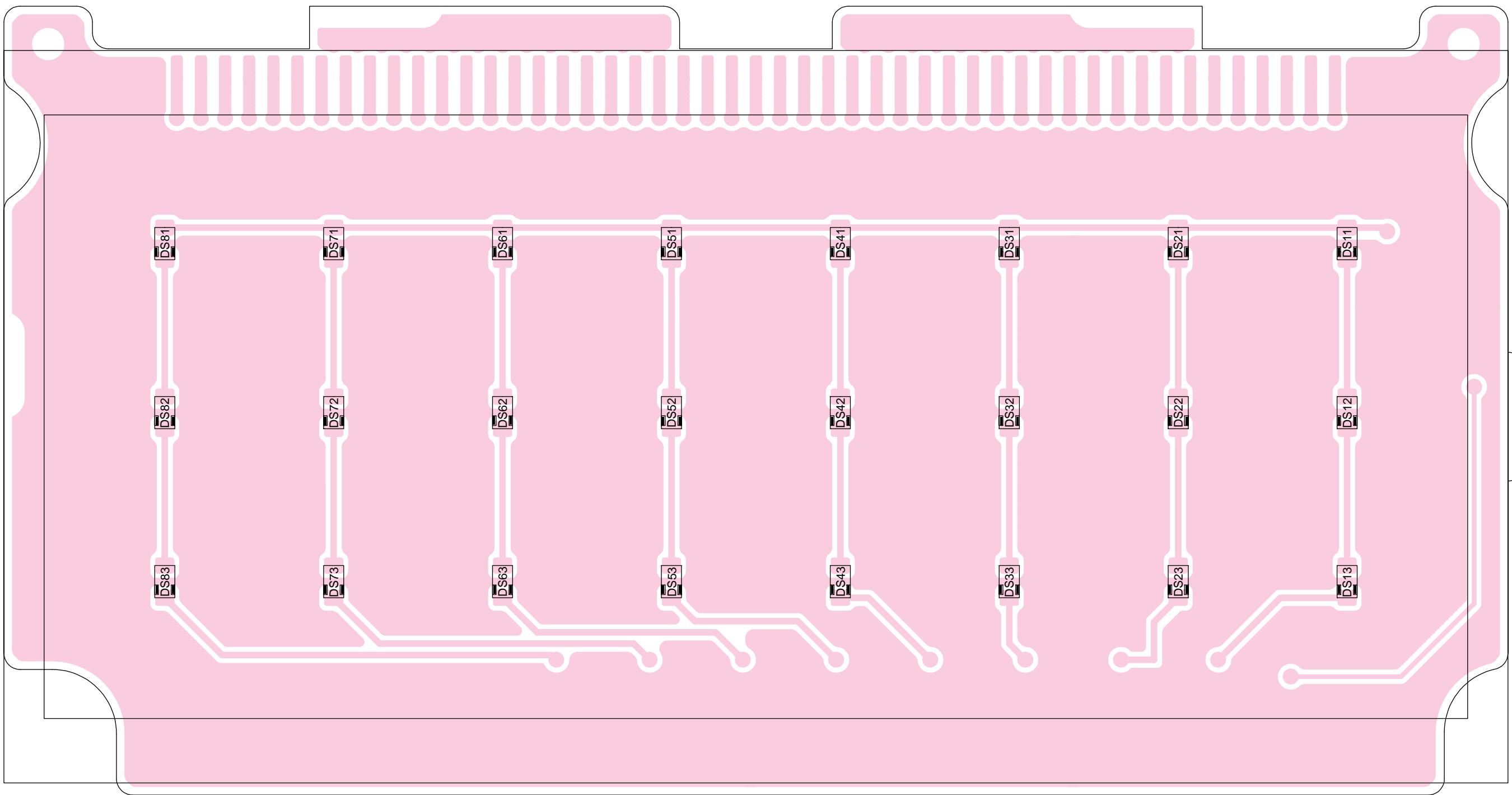


10	GND
	AFE
	AFE
	AFE
	AFE
	ESPO
	ESPO
	ESPO
	AFO
	AFO
1	AFO

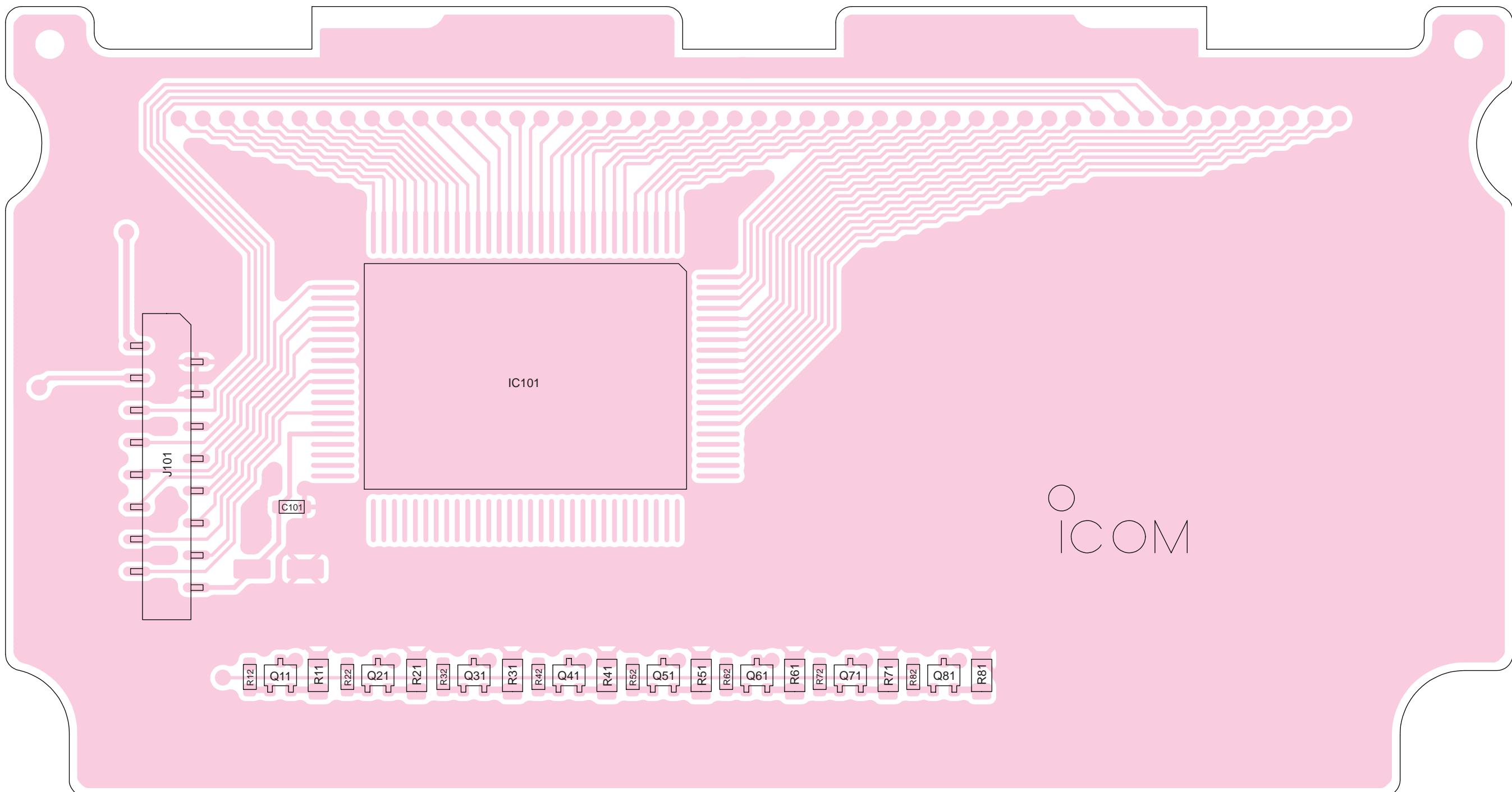
J101  
to LOGIC board J471

## 8-2 DISPLAY BOARD

### • TOP VIEW



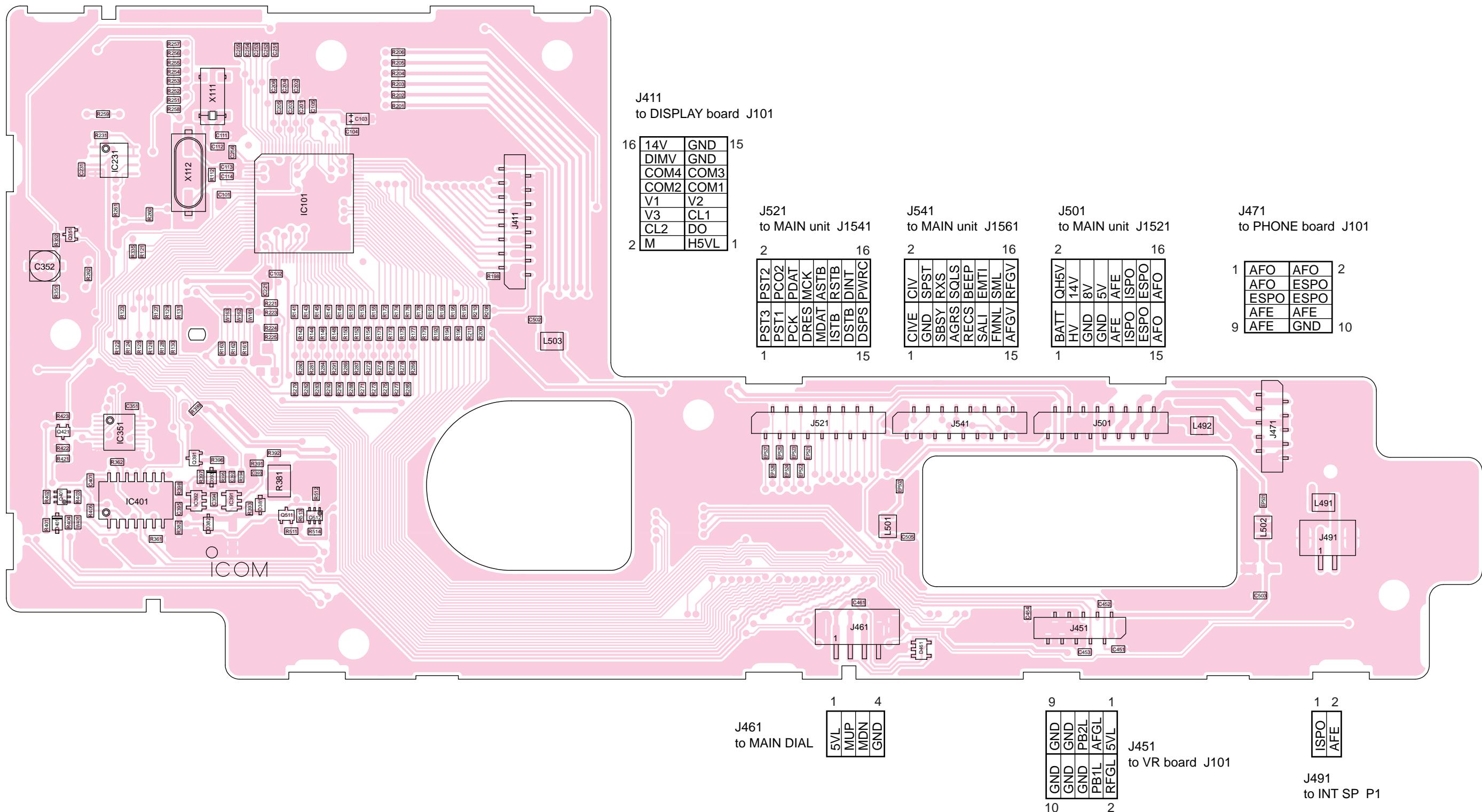
• BOTTOM VIEW



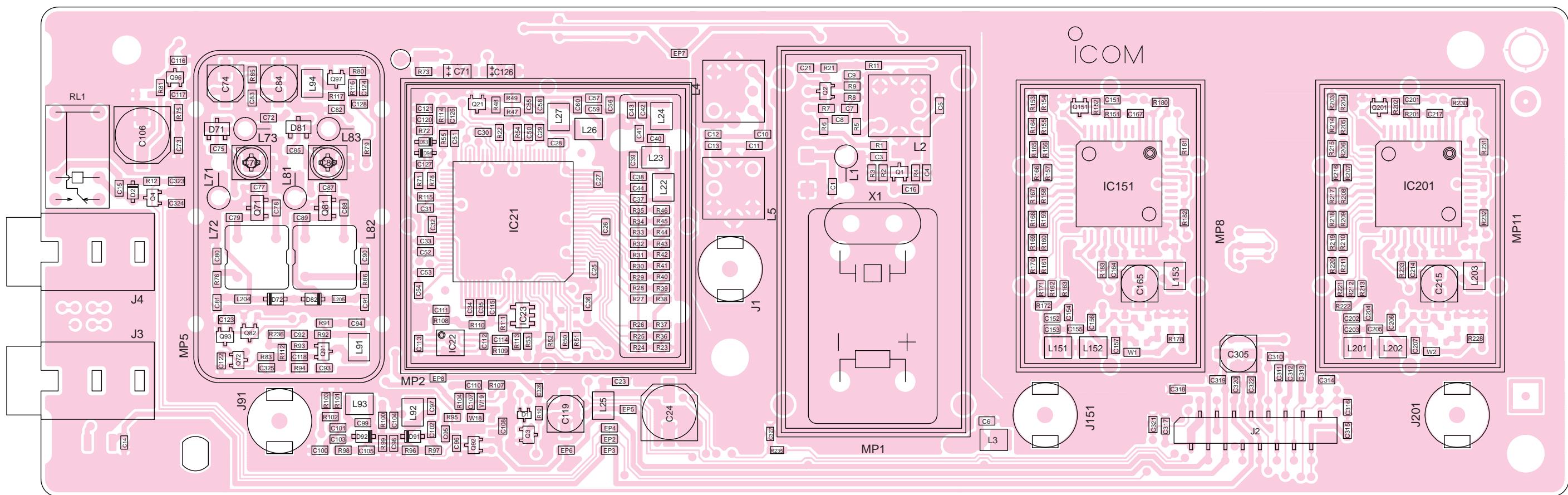
16	14V	GND	15
	DIMV	GND	
	COM4	COM3	
	COM2	COM1	
	V1	V2	
	V3	CL1	
	CL2	DO	
2	M	H5VL	1

J101  
to LOGIC board J411

## 8-3 LOGIC BOARD



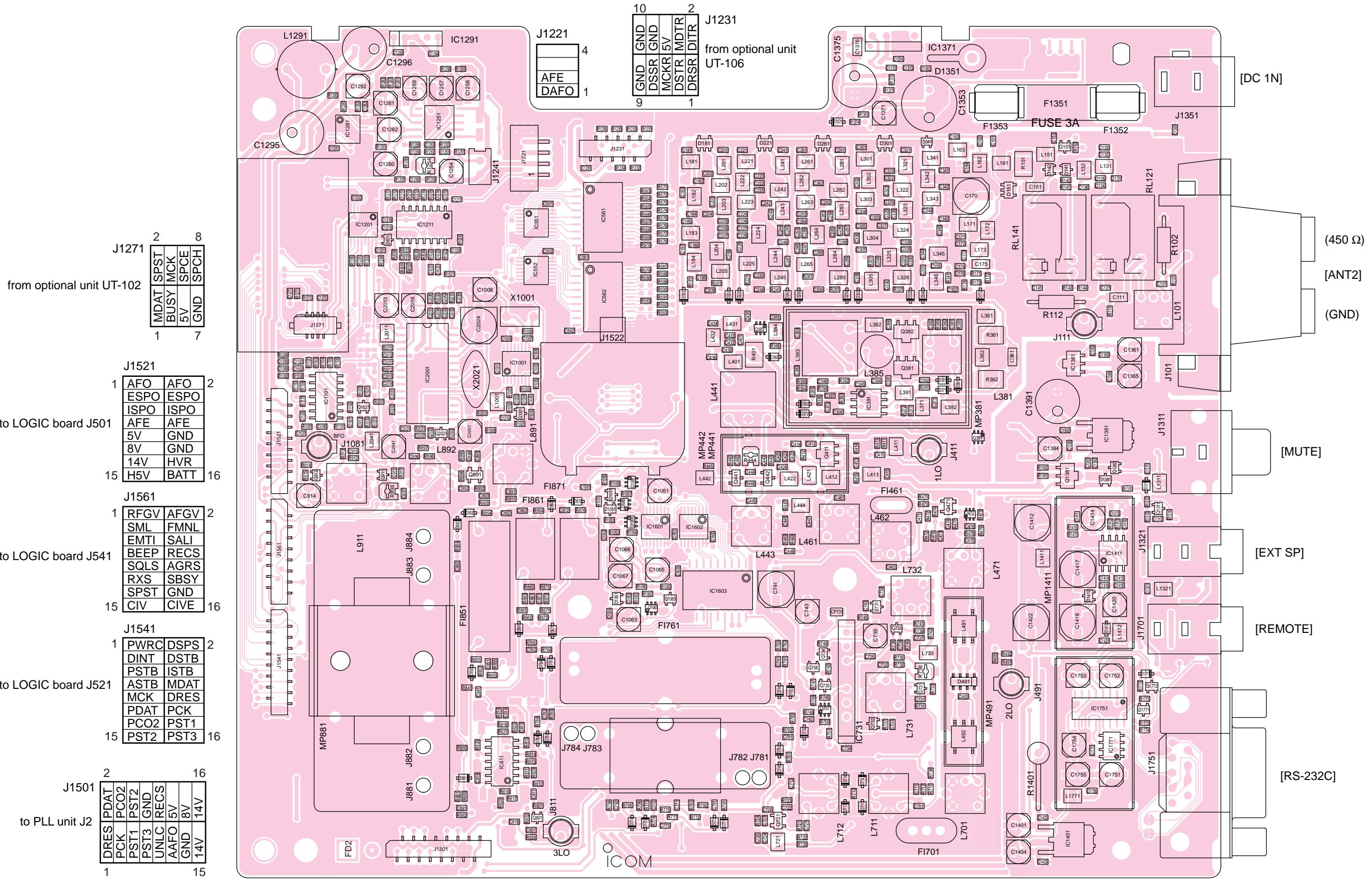
## 8-4 PLL UNIT



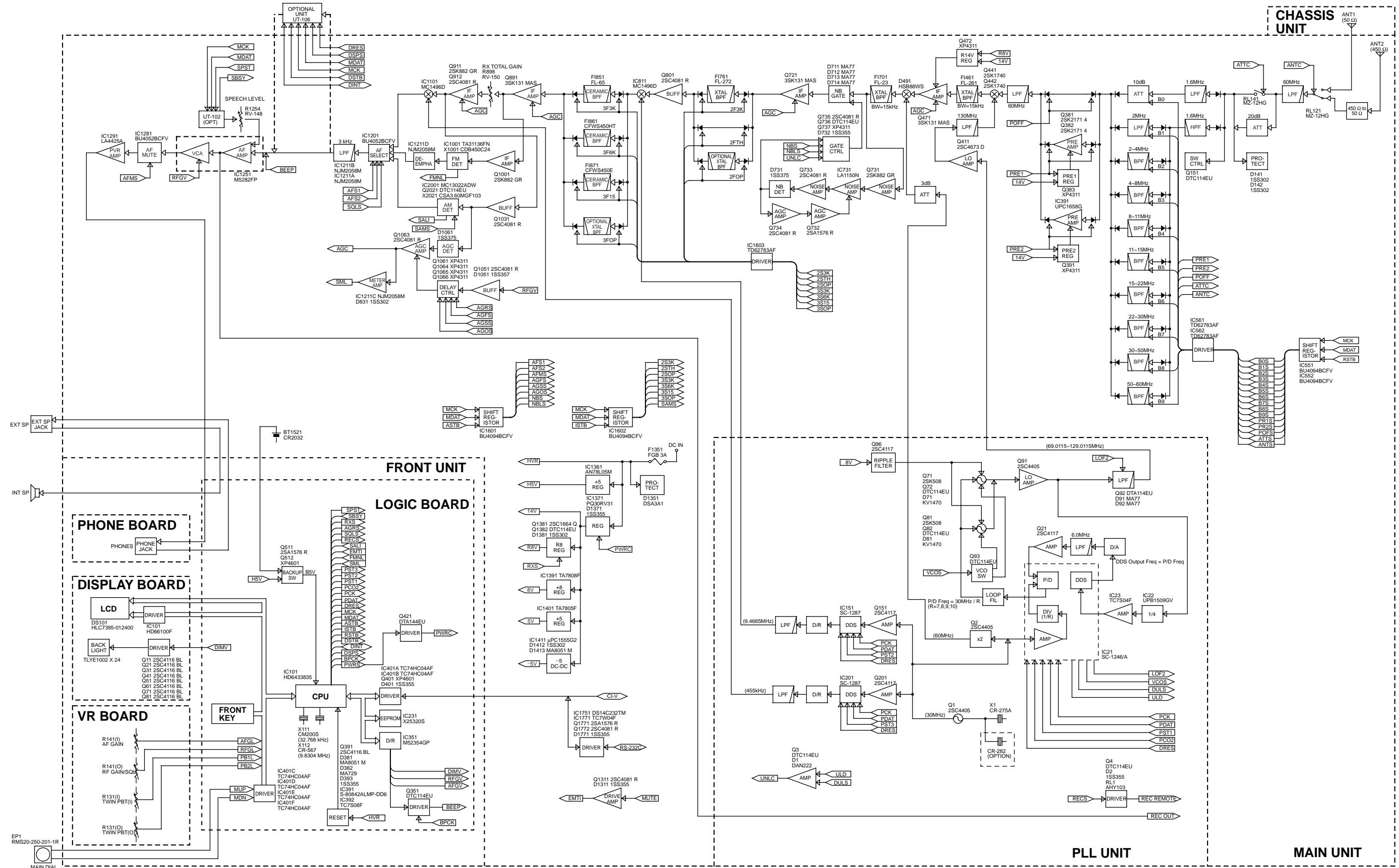
1	14V	14V	2
	8V	GND	
	5V	AAFO	
	RECS	UNLC	
	GND	PST3	16
	PST2	PST1	
	PCO2	PCK	
	PDAT	DRES	

J2  
to MAIN unit J1501

## 8-5 MAIN UNIT

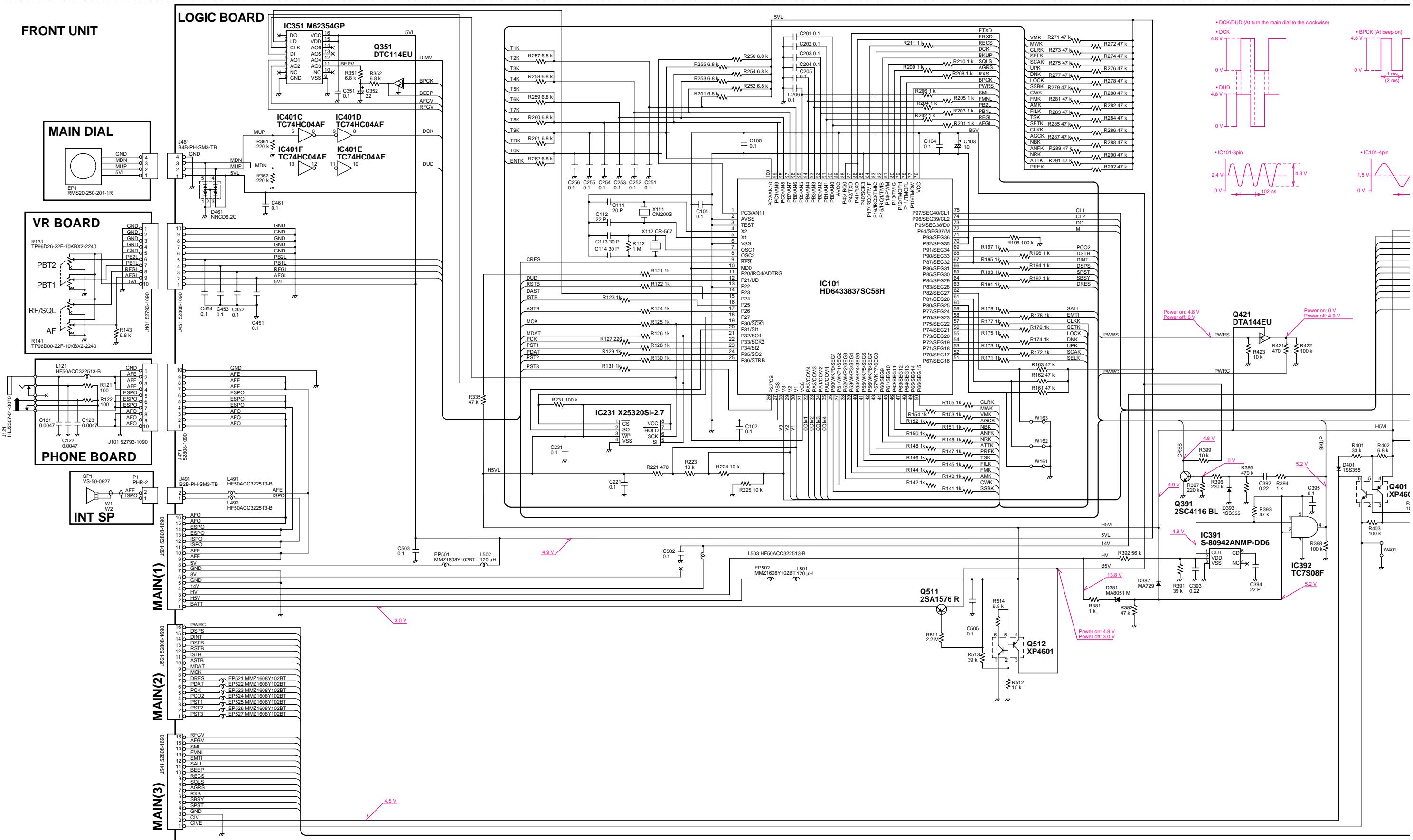


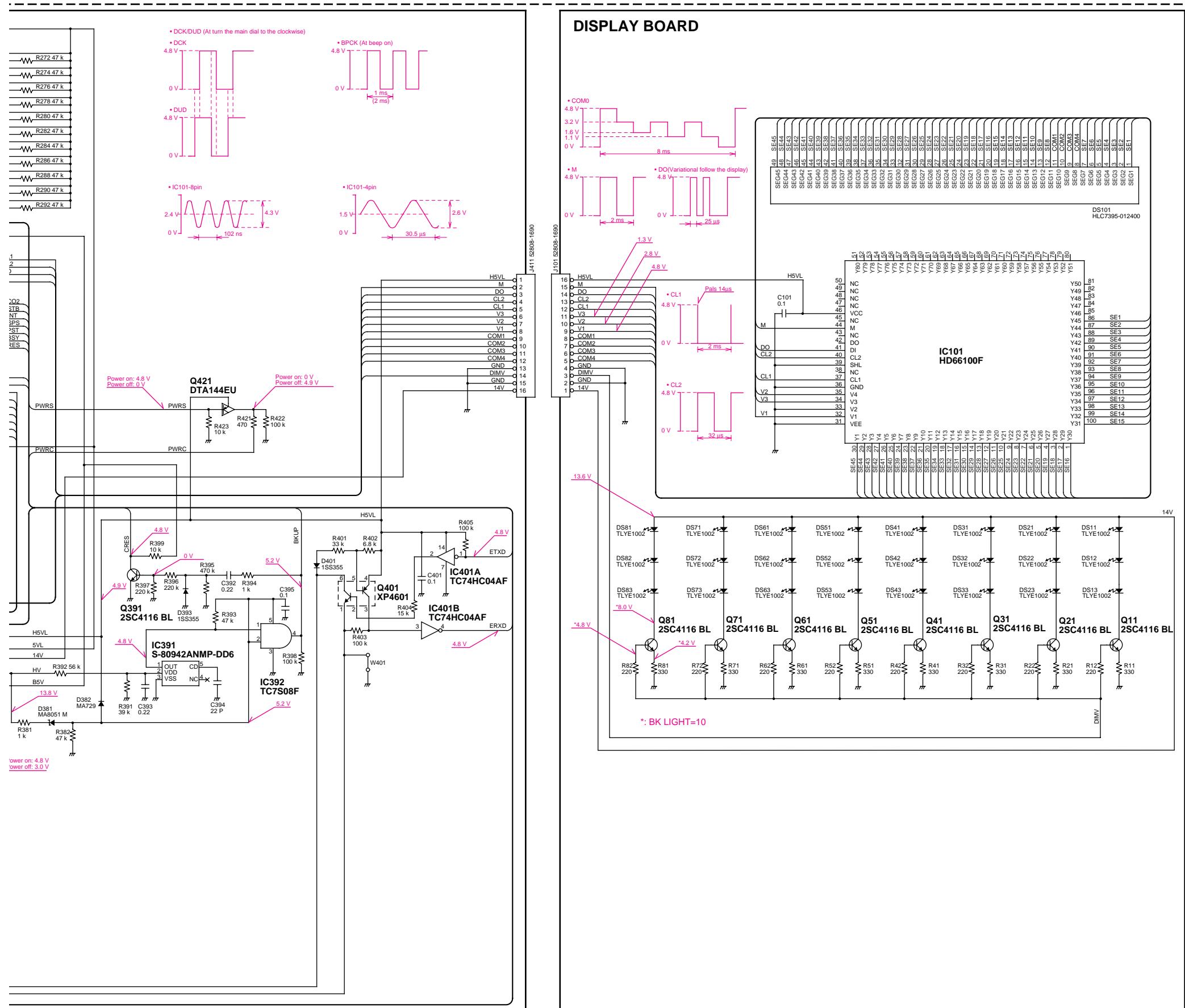
## SECTION 9 BLOCK DIAGRAM



## SECTION 10 VOLTAGE DIAGRAM

### 10-1 FRONT UNIT





COMPLETE VIEW

## SECTION 10 VOLTAGE DIAGRAM

### 10-1 FRONT UNIT

#### FRONT UNIT

##### MAIN DIAL

##### VR BOARD

##### PHONE BOARD

##### MAIN(1)

##### MAIN(2)

##### MAIN(3)

#### LOGIC BOARD

**IC351 MC3254GP**, **Q351 DTC114EU**, **IC401C TC74HC04AF**, **IC401D TC74HC04AF**

**IC101 HD6433837SC58H**

#### DISPLAY BOARD

**DS101 HLC7395-012400**

**IC101 HD66100F**

**Q421 DT144EU**

**IC391 2SC4116 BL**

**IC401A TC74HC04AF**

**IC401B TC74HC04AF**

**Q81 2SC4116 BL**

**Q71 2SC4116 BL**

**Q61 2SC4116 BL**

**Q51 2SC4116 BL**

**Q41 2SC4116 BL**

**Q21 2SC4116 BL**

**Q11 2SC4116 BL**

**DS31 TLVE100Z**

**DS32 TLVE100Z**

**DS33 TLVE100Z**

**DS34 TLVE100Z**

**DS35 TLVE100Z**

**DS36 TLVE100Z**

**DS37 TLVE100Z**

**DS38 TLVE100Z**

**DS39 TLVE100Z**

**DS40 TLVE100Z**

**DS41 TLVE100Z**

**DS42 TLVE100Z**

**DS43 TLVE100Z**

**DS44 TLVE100Z**

**DS45 TLVE100Z**

**DS46 TLVE100Z**

**DS47 TLVE100Z**

**DS48 TLVE100Z**

**DS49 TLVE100Z**

**DS50 TLVE100Z**

**DS51 TLVE100Z**

**DS52 TLVE100Z**

**DS53 TLVE100Z**

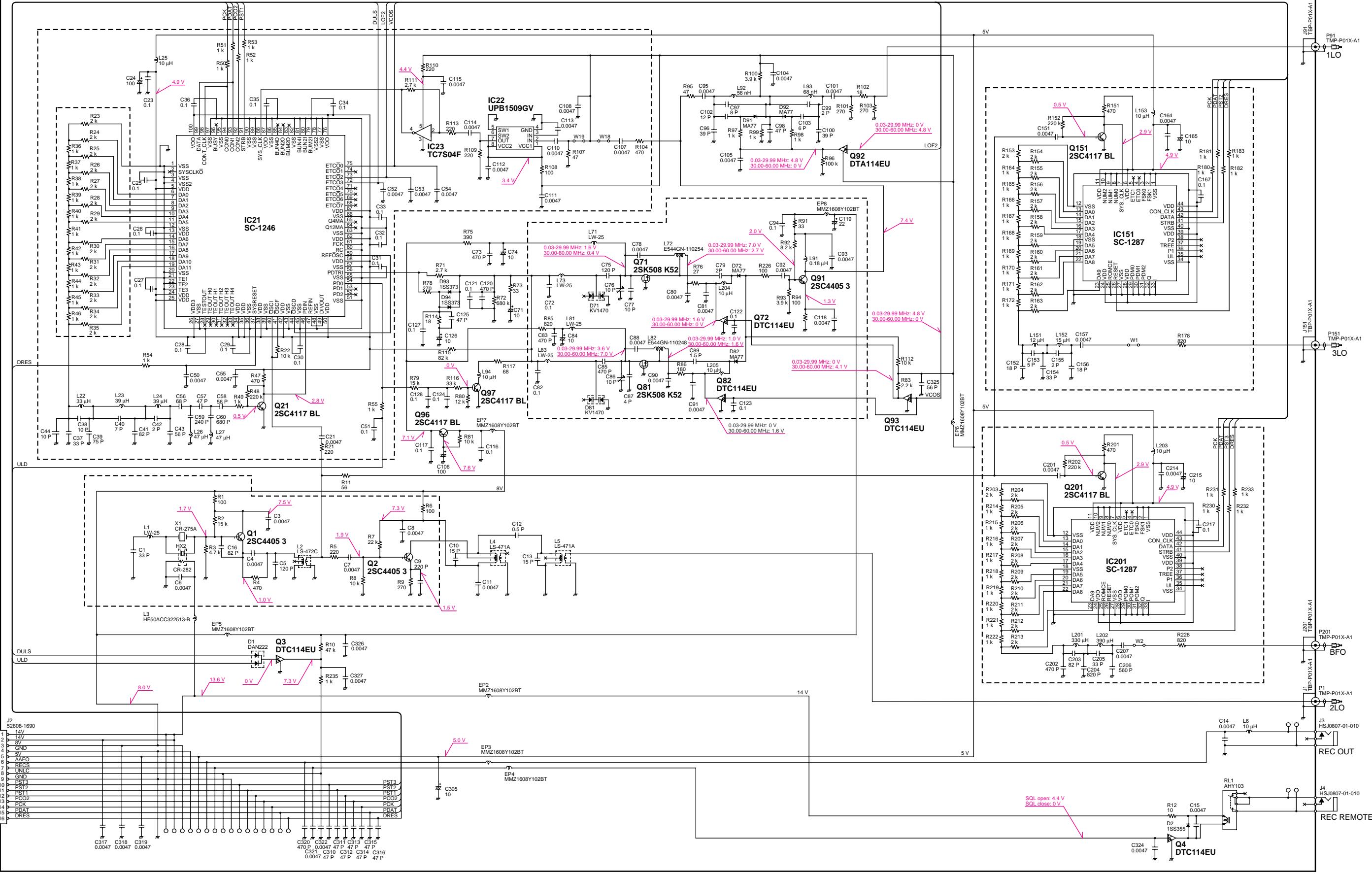
**DS54 TLVE100Z**

**DS55 TLVE100Z**

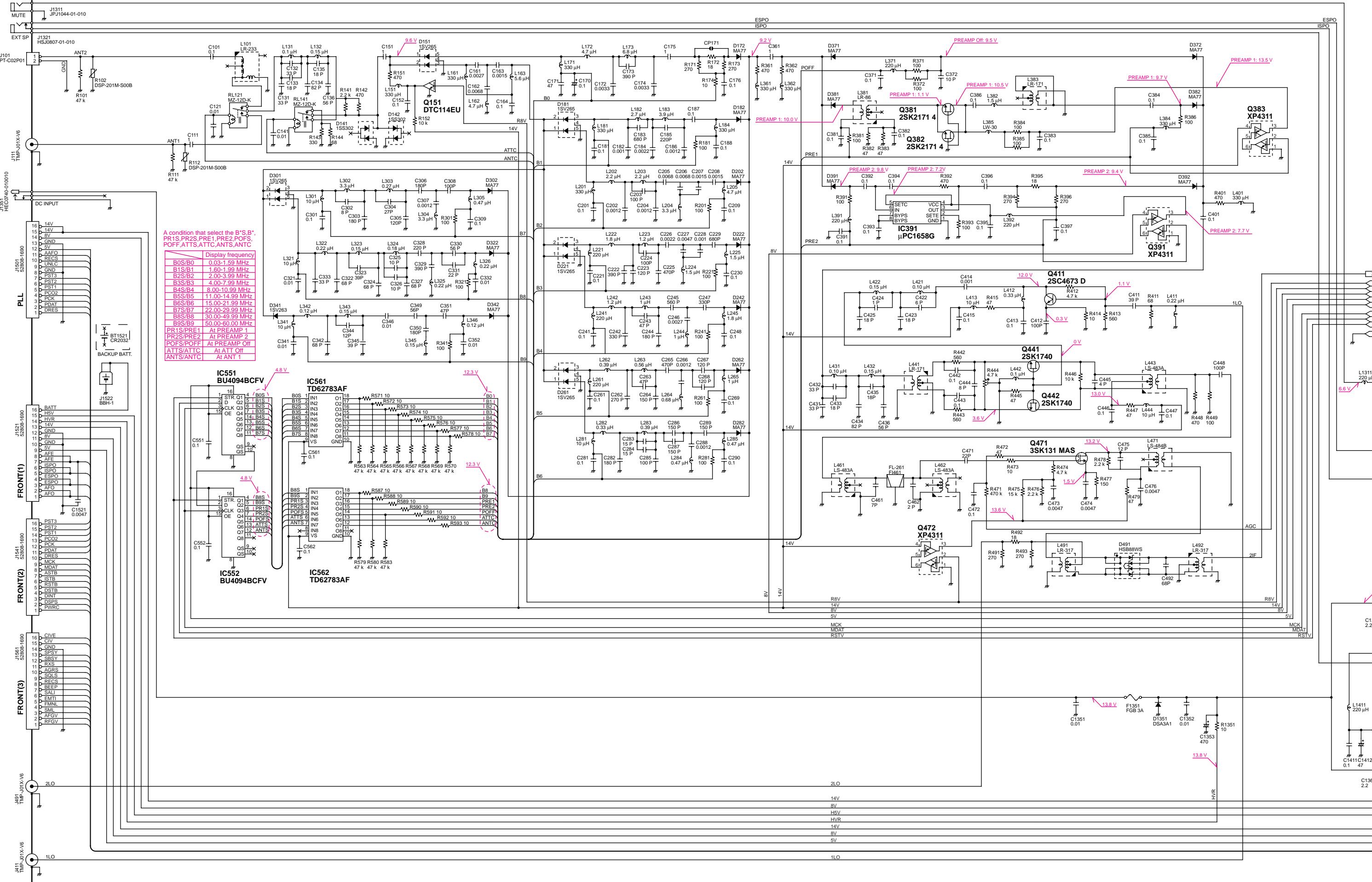
**DS56 TLVE100Z**

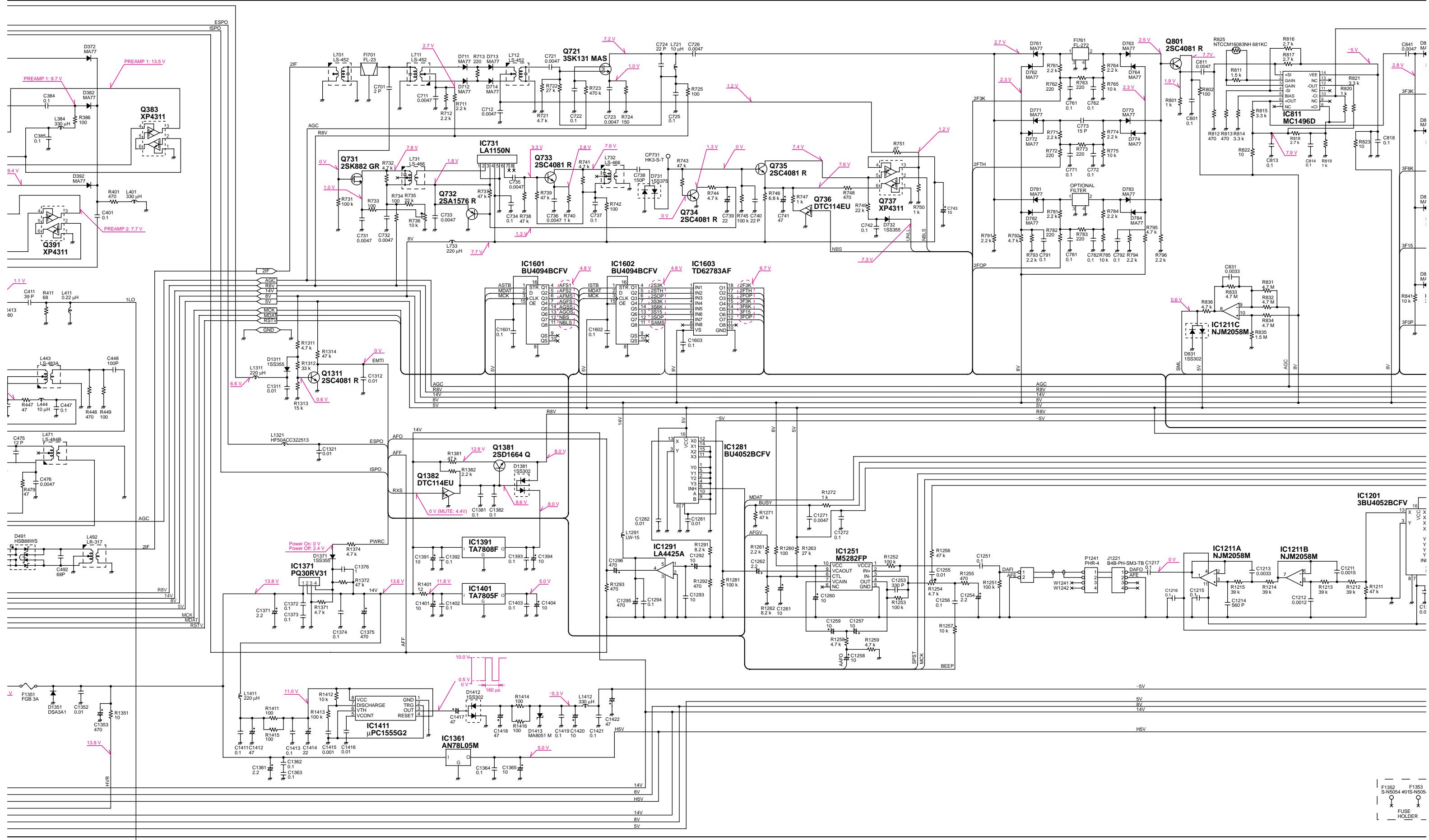
## 10-2 PLL UNIT

### PLL UNIT



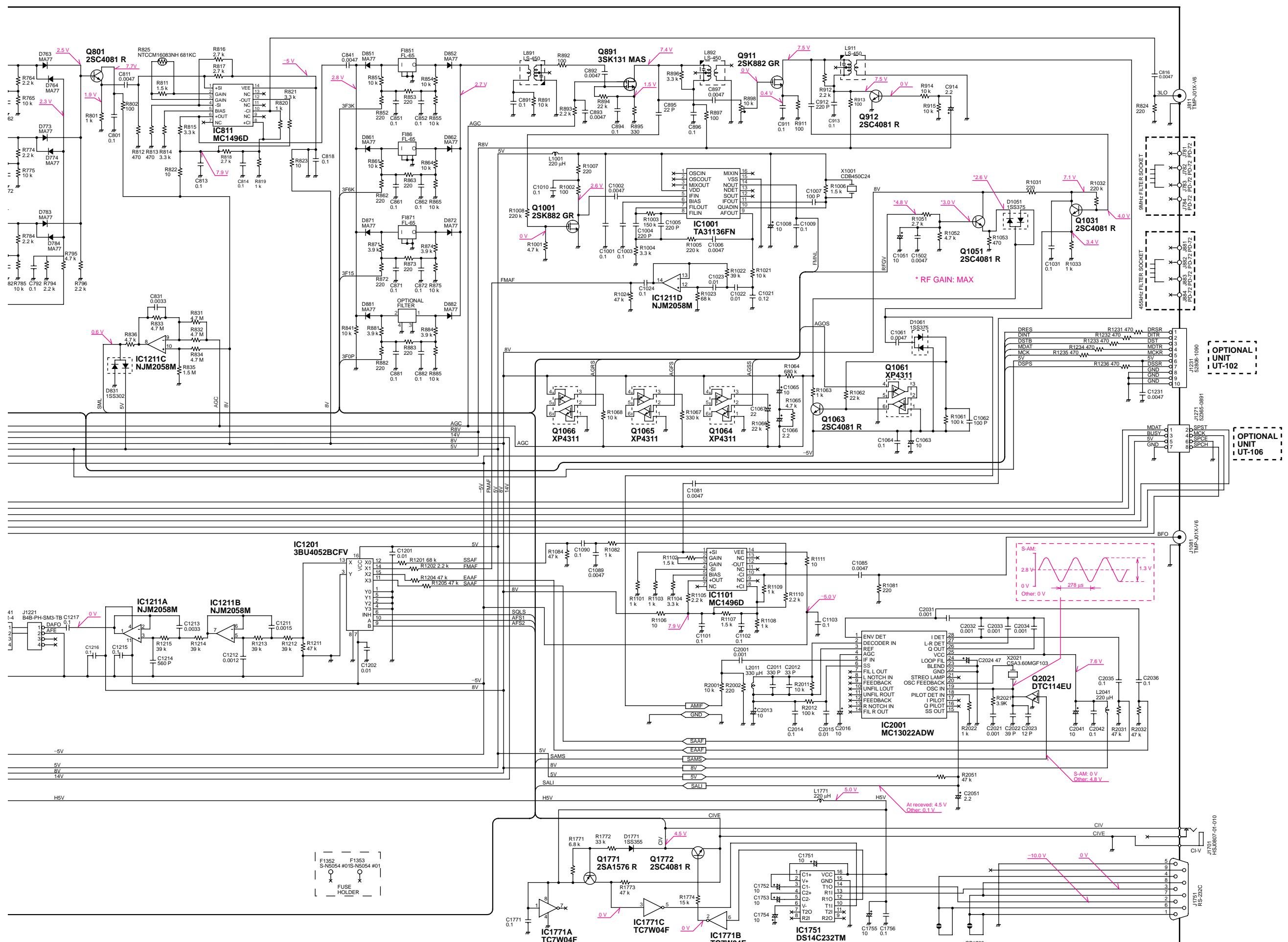
## 10-3 MAIN UNIT





COMPLETE VIEW

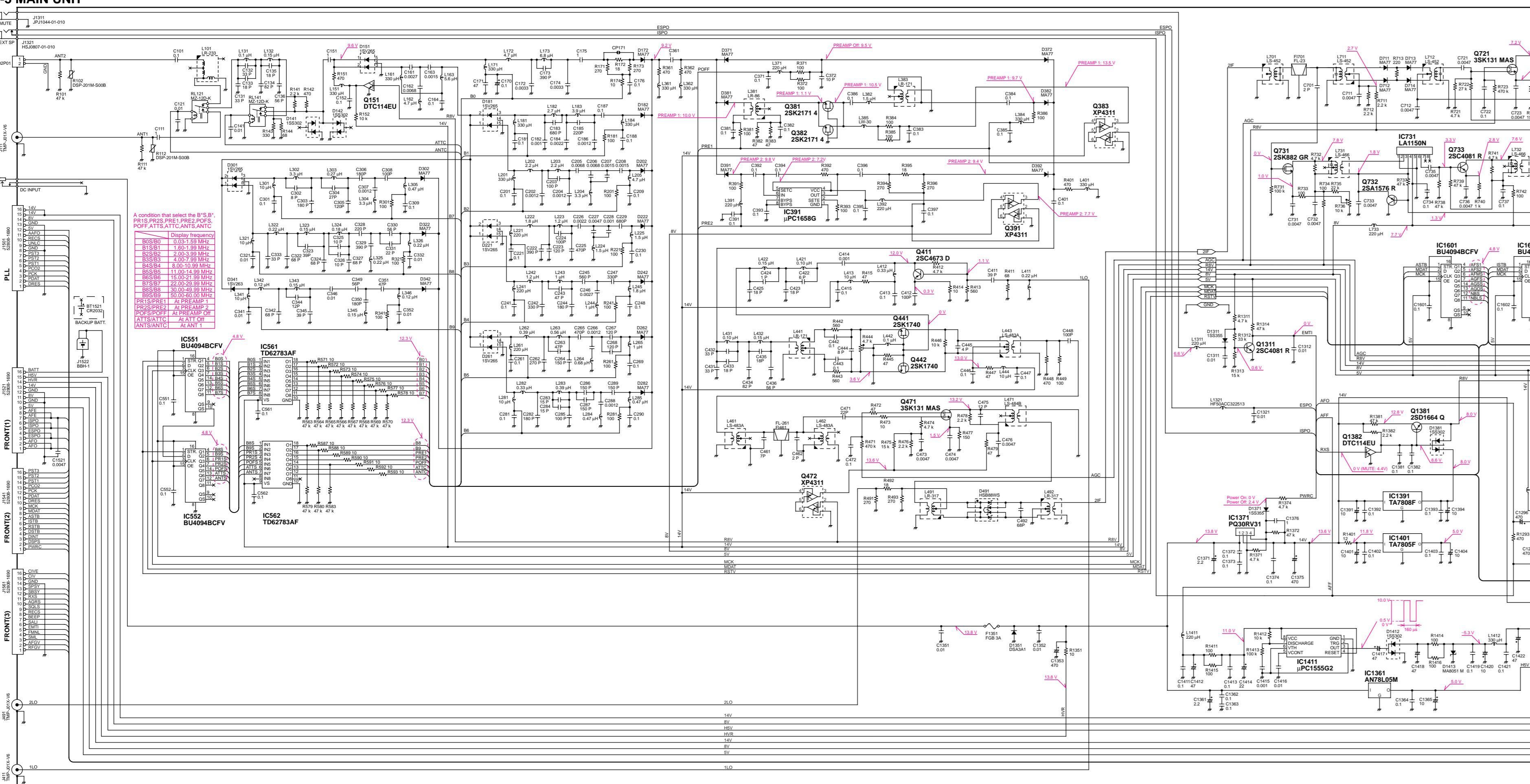




COMPLETE VIEW

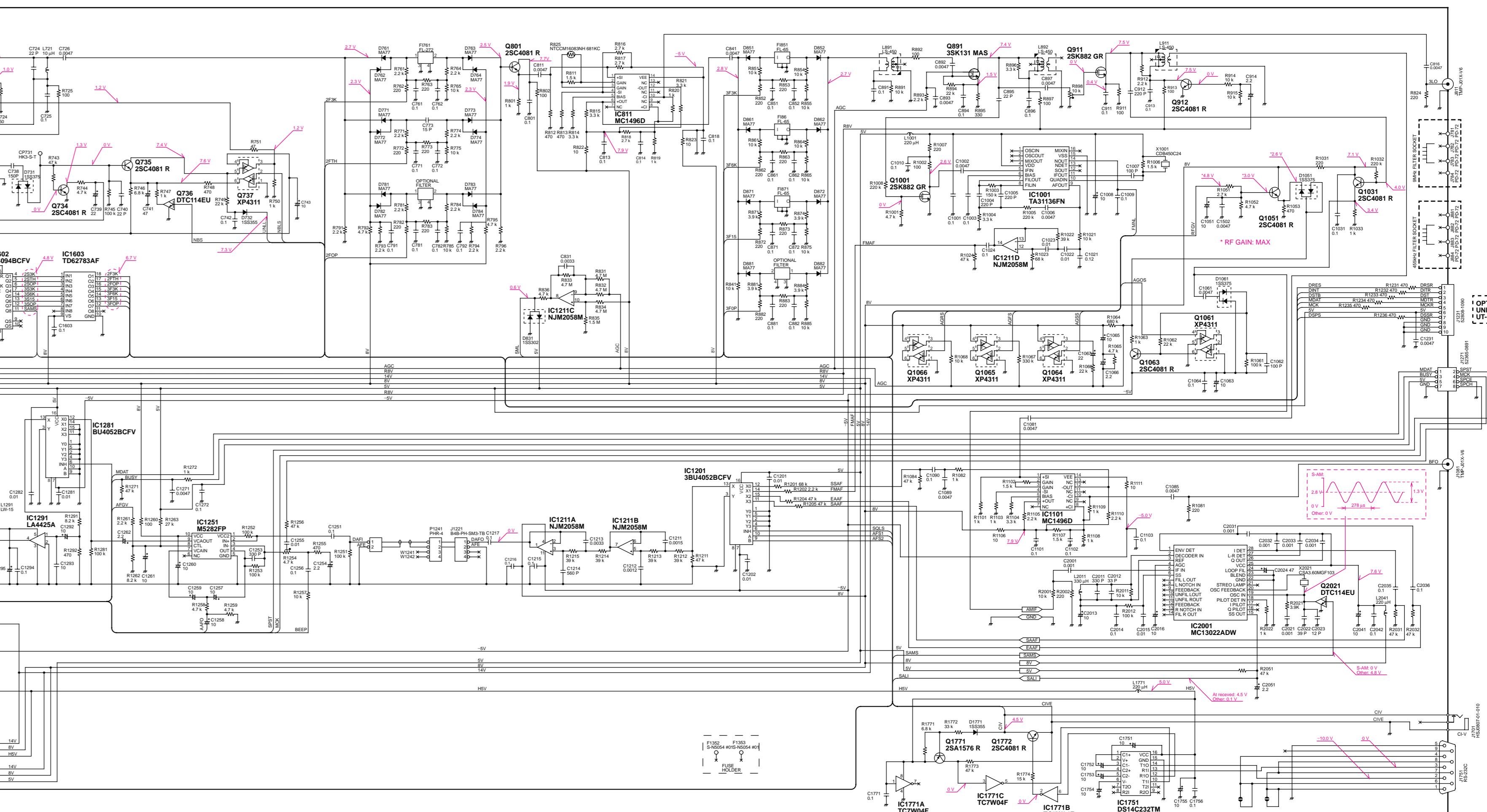


## 10-3 MAIN UNIT



LEFT SIDE

10 - 3



CENTER

10 - 4

RIGHT SIDE

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